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Ebisuno et al.

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(45) Date of Patent: *Nov. 10, 2015

(54) **DISPLAY DEVICE**

(71) Applicant: **JOLED INC.**, Tokyo (JP)

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(73) Assignee: **JOLED INC.**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 337 days.

This patent is subject to a terminal disclaimer.

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(65) **Prior Publication Data**

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Related U.S. Application Data

(63) Continuation of application No. PCT/JP2011/003424, filed on Jun. 16, 2011.

(51) **Int. Cl.**

G09G 3/30	(2006.01)
H05B 33/08	(2006.01)
G09G 3/32	(2006.01)

(52) **U.S. Cl.**

CPC ***H05B 33/08*** (2013.01); ***G09G 3/3225*** (2013.01); ***G09G 3/3275*** (2013.01); *G09G 2320/029* (2013.01); *G09G 2320/0223* (2013.01); *G09G 2320/0233* (2013.01); *G09G 2330/028* (2013.01)

(58) **Field of Classification Search**

CPC G09G 2330/021; G09G 3/3233; H05B 33/0815

USPC 345/76, 80, 211–212; 315/291, 294, 315/297, 307

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,518,962	B2	2/2003	Kimura et al.
7,362,322	B2	4/2008	Kimura et al.

(Continued)

FOREIGN PATENT DOCUMENTS

CN	101515435	8/2009
CN	101273398 B	6/2011

(Continued)

OTHER PUBLICATIONS

Extended European Search Report from the European Patent Office (E.P.O.), mailed Jun. 17, 2014, for the related European Patent Application No. 11846054.2.

(Continued)

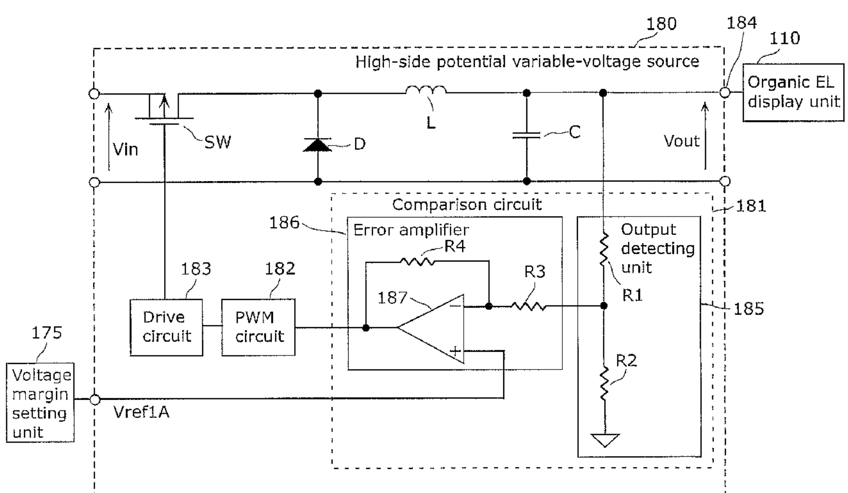
Primary Examiner — Jason M Crawford

(74) *Attorney, Agent, or Firm* — Greenblum & Bernstein, P.L.C.

(57) **ABSTRACT**

A display device includes: a high-side potential variable-voltage source which outputs a high-side output potential and a low-side potential variable-voltage source which outputs a low-side output potential; an organic EL display unit in which pixels are arranged; a high-side potential difference detecting circuit which detects a high-side potential applied to a first pixel and a low-side potential difference detecting circuit which detects a low-side potential applied to a second pixel; a high-side potential voltage margin setting unit and a low-side potential voltage setting unit which regulate the output potential of the high-side potential variable-voltage source and the low-side potential variable-voltage source to set a potential difference between the high-side potential of the first pixel and a reference potential to a predetermined potential difference and set a potential difference between the low-side potential of the second pixel and a reference potential to a predetermined potential difference; and a signal processing circuit.

13 Claims, 25 Drawing Sheets



(56) **References Cited**

U.S. PATENT DOCUMENTS

7,864,172	B2	1/2011	Miyake et al.	
7,973,745	B2	7/2011	Mizukoshi et al.	
8,089,428	B2	1/2012	Yaguchi et al.	
8,159,421	B2	4/2012	Hwang et al.	
8,194,013	B2	6/2012	Choi	
8,547,307	B2	10/2013	Shirouzu et al.	
8,803,869	B2 *	8/2014	Kato et al.	345/212
8,941,638	B2 *	1/2015	Ebisuno et al.	345/212
8,952,952	B2 *	2/2015	Ebisuno et al.	345/212
8,952,953	B2 *	2/2015	Ebisuno et al.	345/212
2001/0043168	A1	11/2001	Koyama et al.	
2002/0180721	A1	12/2002	Kimura et al.	
2003/0063081	A1	4/2003	Kimura et al.	
2004/0070331	A1	4/2004	Kuno et al.	
2006/0038501	A1	2/2006	Koyama et al.	
2006/0077137	A1	4/2006	Kwon	
2006/0176253	A1	8/2006	Yazawa et al.	
2007/0080905	A1	4/2007	Takahara	
2007/0145902	A1	6/2007	Yaguchi et al.	
2008/0180365	A1	7/2008	Ozaki	
2008/0186297	A1	8/2008	Morita	
2008/0266216	A1 *	10/2008	Choi	345/77
2008/0291135	A1	11/2008	Kim et al.	
2008/0297055	A1	12/2008	Miyake et al.	
2009/0026969	A1	1/2009	Joo	
2009/0207105	A1	8/2009	Hwang et al.	
2009/0207106	A1	8/2009	Mizukoshi et al.	
2009/0303162	A1	12/2009	Kohno et al.	
2010/0103203	A1	4/2010	Choi	
2010/0110059	A1	5/2010	Kang et al.	
2010/0214273	A1	8/2010	Shirouzu et al.	
2010/0259528	A1 *	10/2010	Smith et al.	345/212
2011/0157134	A1 *	6/2011	Ogura	345/211
2011/0169798	A1	7/2011	Lee et al.	
2011/0242087	A1 *	10/2011	Ebisuno et al.	345/212
2011/0255586	A1	10/2011	Li et al.	
2012/0320024	A1	12/2012	Ebisuno et al.	
2012/0327063	A1 *	12/2012	Izawa et al.	345/212
2013/0016091	A1	1/2013	Kato et al.	
2013/0285889	A1	10/2013	Shirouzu et al.	

FOREIGN PATENT DOCUMENTS

EP	2284825	2/2011
JP	2003-280590	10/2003
JP	2004-246250	9/2004
JP	2006-065148	3/2006
JP	2006-251602	9/2006
JP	2007-121430	5/2007
JP	2008-268914	11/2008
JP	2008-299019	12/2008
JP	2009-198691	9/2009
JP	2009-294376	12/2009
JP	2010-199501	9/2010
KR	10-2010-0045055	5/2010
WO	98/40871	9/1998
WO	2010/001590	1/2010
WO	2011/086597	7/2011
WO	2012/172607	12/2012
WO	2012/176241	12/2012
WO	2013/008271	1/2013
WO	2013/008272	1/2013

OTHER PUBLICATIONS

Extended European Search Report from the European Patent Office, mailed Oct. 29, 2014, in related European Patent Application No. 11869299.5.
China Office Action with Search Report (including English language translation of Search Report), mailed Feb. 10, 2015, for related Chinese Patent Application No. 201180004566.6.
Office Action, mailed Aug. 13, 2014, in related U.S. Appl. No. 13/467,462.
Office Action, mailed Feb. 24, 2014, in related U.S. Appl. No. 13/467,462.
International Search Report for related International Application PCT/JP2010/000149, mailed Feb. 9, 2010.
International Search Report for related International Application PCT/JP2011/003424, mailed Sep. 27, 2011.
International Search Report for related International Application PCT/JP2011/003432, mailed Sep. 27, 2011.
International Search Report for related International Application PCT/JP2011/003979, mailed Aug. 16, 2011.
International Search Report for related International Application PCT/JP2011/003609, mailed Sep. 20, 2011.
International Search Report for related International Application PCT/JP2011/003989, mailed Aug. 9, 2011.
Official Action in related U.S. Appl. No. 13/157,577, mailed Jan. 24, 2013.
Office Action in U.S. Appl. No. 13/467,462, mailed Aug. 28, 2013.
U.S. Office Action, mailed Sep. 11, 2013, in related U.S. Appl. No. 13/157,577.
Extended European Search Report from the European Patent Office, mailed Oct. 9, 2014, in related European Patent Application No. 11867592.5.
Japan Office Action, mailed Nov. 26, 2013, in the corresponding Japanese Application 2010-525132.
Japan Office Action, mailed Mar. 24, 2015, in related Japanese Patent Application No. 2012-502383.
Chinese Office Action, mailed May 28, 2015, in corresponding Chinese Patent Application No. 201180032663.6 (including English language translation of Search Report).
Korean Office Action, mailed Sep. 10, 2015, in related Korean Patent Application No. 10-2010-7016548.

* cited by examiner

FIG. 1

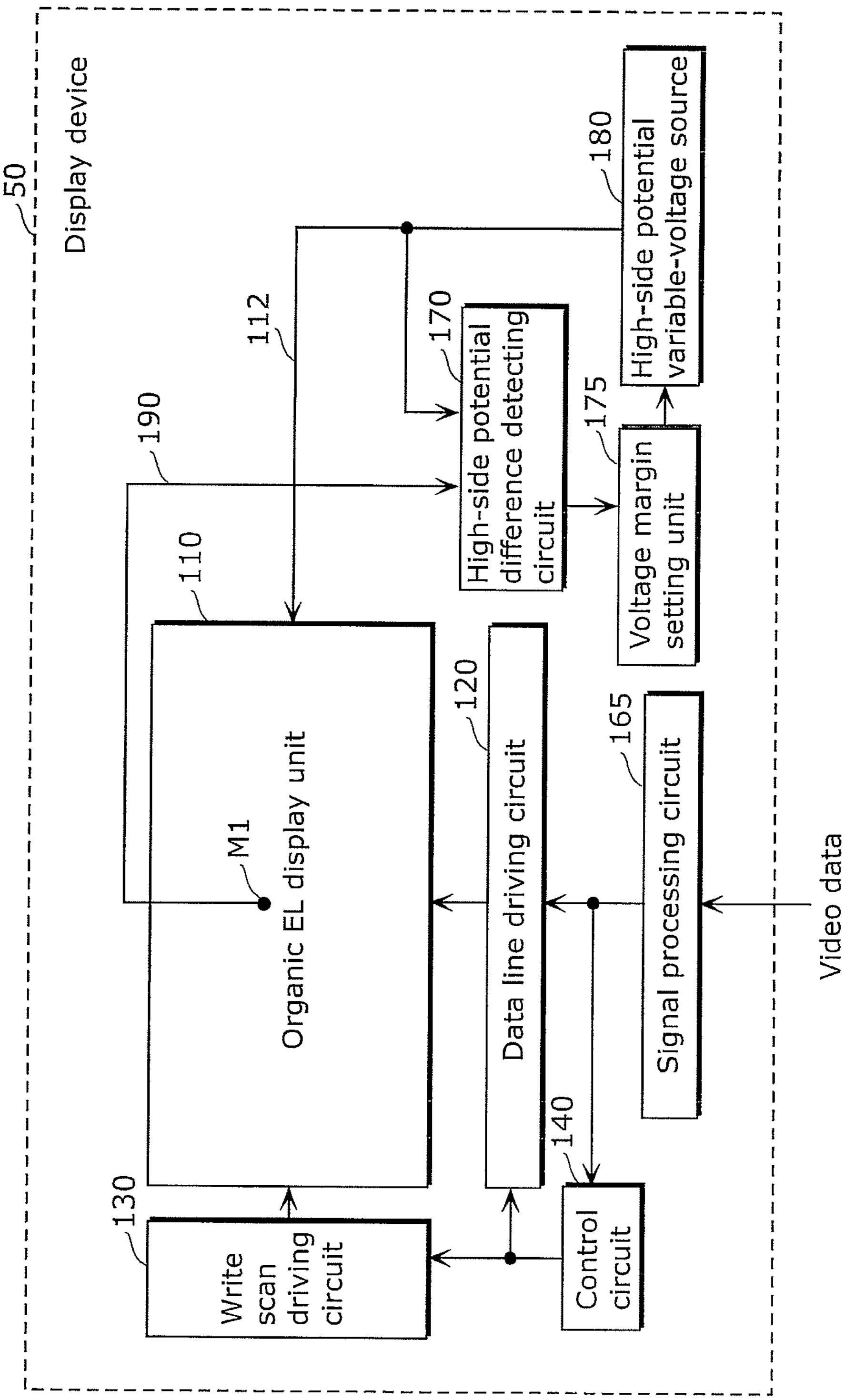

50
Display device
180
High-side potential variable-voltage source
170
High-side potential difference detecting circuit
175
Voltage margin setting unit
112
190
110
Organic EL display unit
M1
120
Data line driving circuit
165
Signal processing circuit
Video data
130
Write scan driving circuit
140
Control circuit

FIG. 2

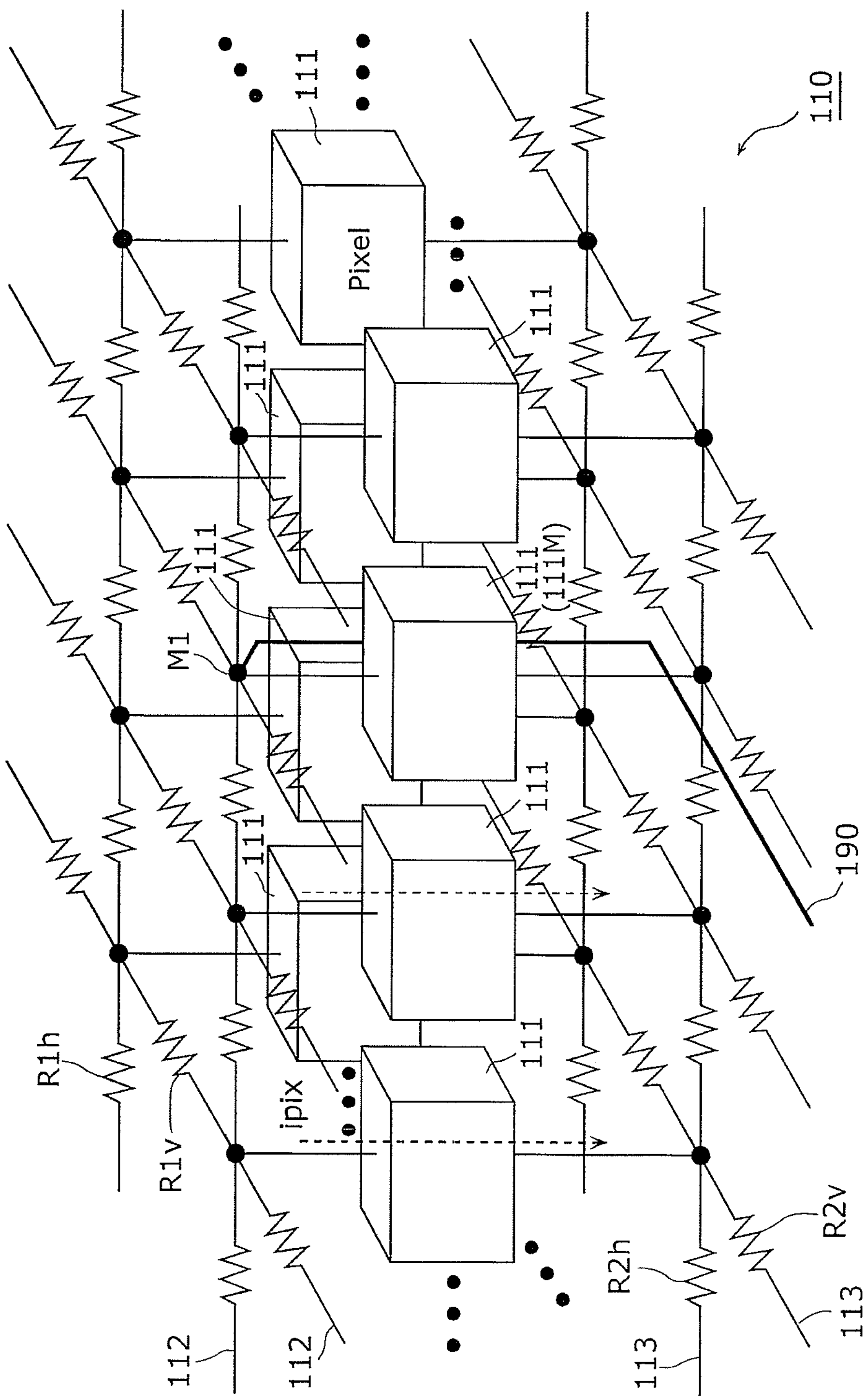


FIG. 3

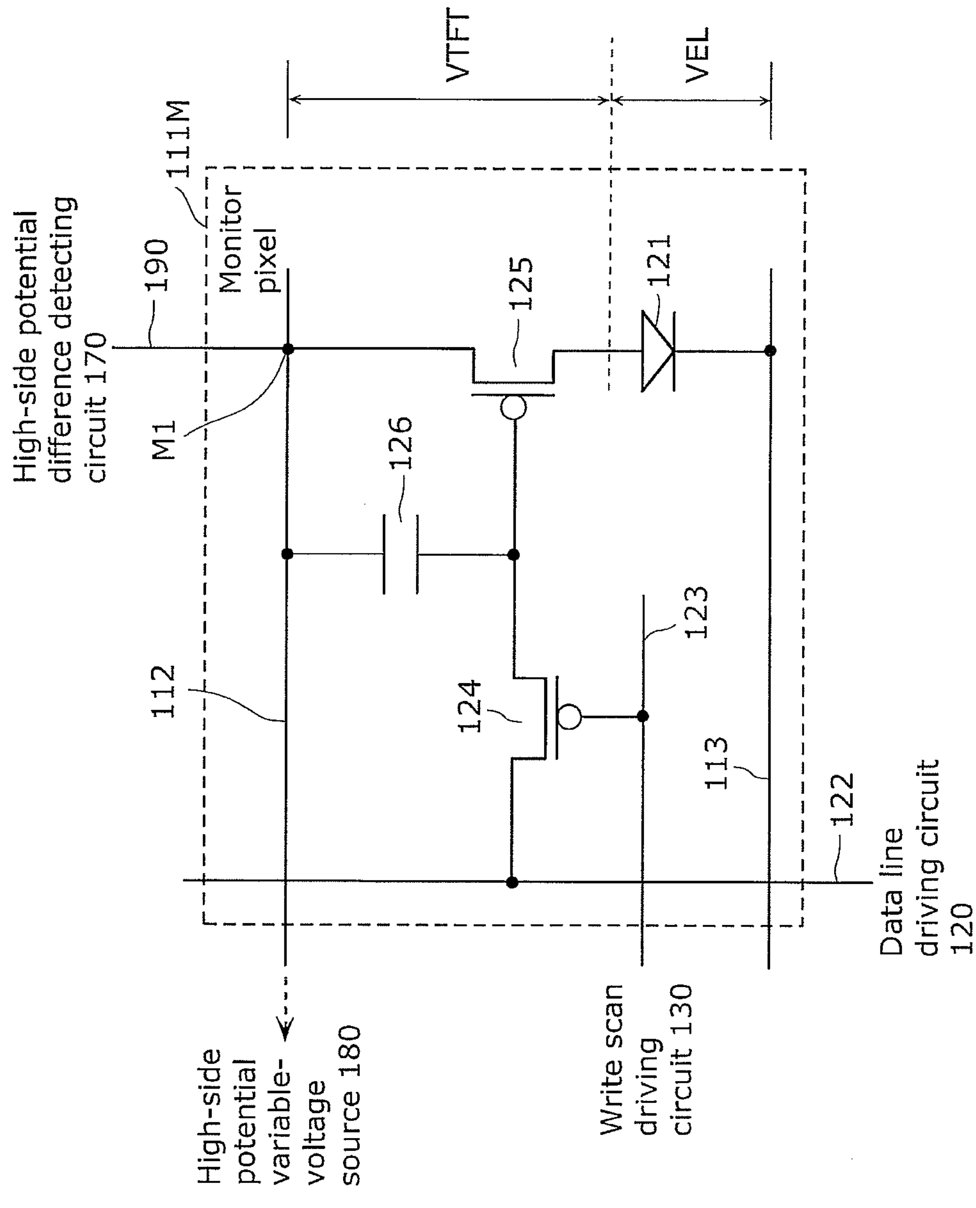
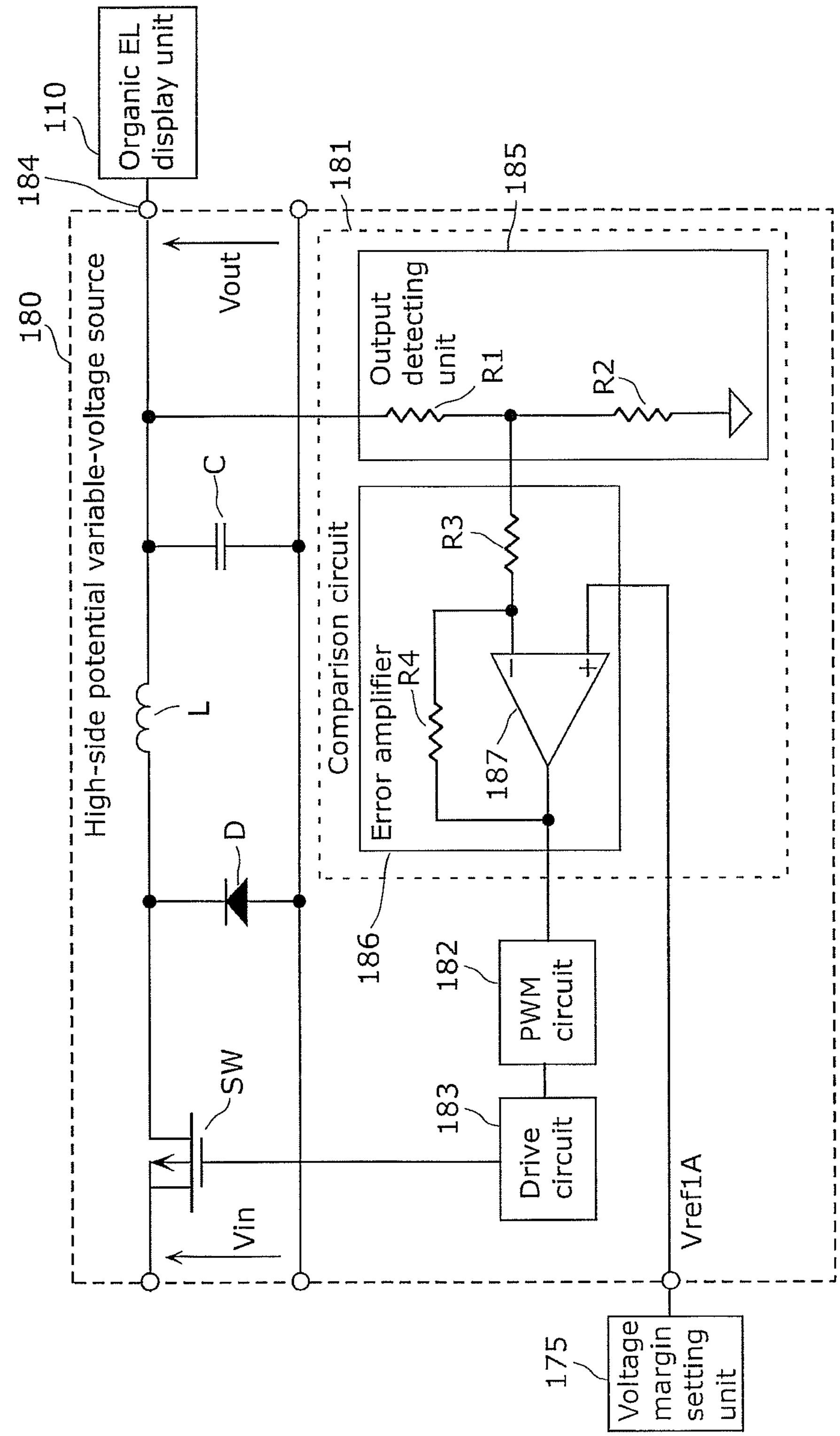

High-side potential difference detecting circuit 170
190
111M
Monitor pixel
M1
VTFT
VEL
125
121
126
123
124
112
113
122
Data line driving circuit 120
High-side potential variable-voltage source 180
Write scan driving circuit 130

FIG. 4



Organic EL display unit
110
184
180
181
185
High-side potential variable-voltage source
Vout
Output detecting unit
R1
R2
C
R3
Comparison circuit
Error amplifier
R4
187
L
D
186
182
PWM circuit
183
Drive circuit
SW
Vin
Vref1A
175
Voltage margin setting unit

FIG. 5

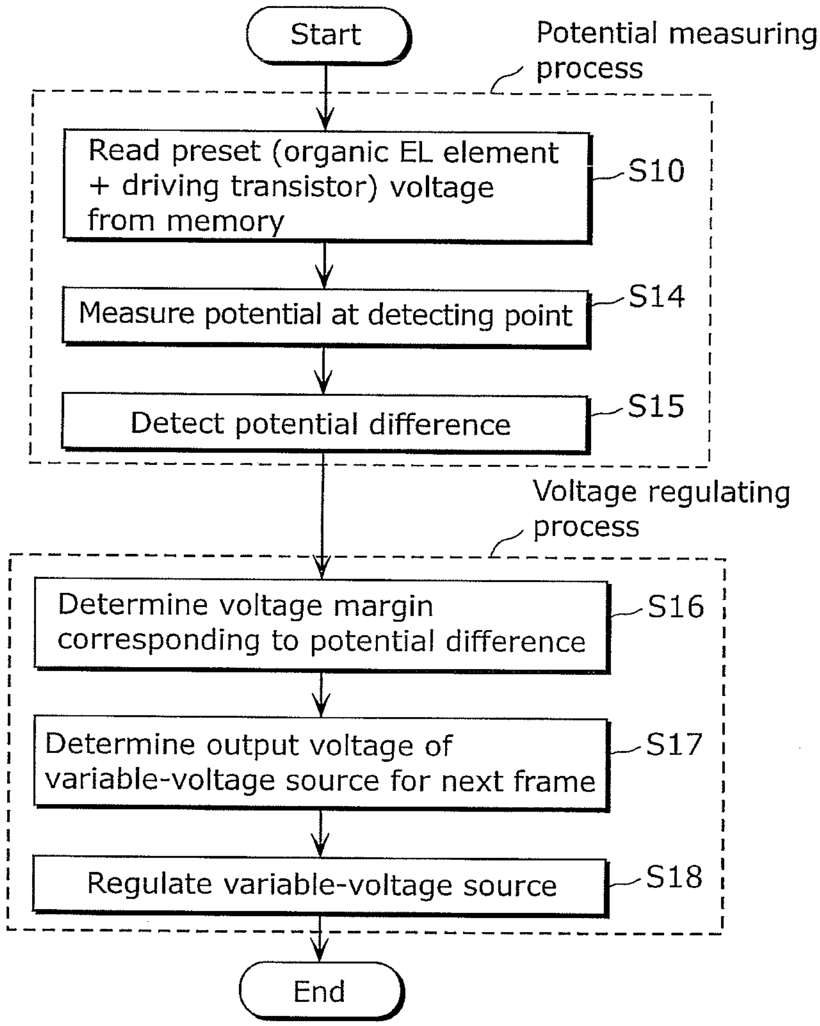


FIG. 6

Video data (Gradation level)	Required voltage (Red)	Required voltage (Green)	Required voltage (Blue)
255	11.2	12.2	8.4

FIG. 7

Potential difference value [V]	Voltage drop margin
0.0	0.0
0.2	0.2
0.4	0.4
0.6	0.6
⋮	⋮
3.4	3.4
3.6	3.6
⋮	⋮
5.6	5.6
5.8	5.8
6.0	6.0

FIG. 8

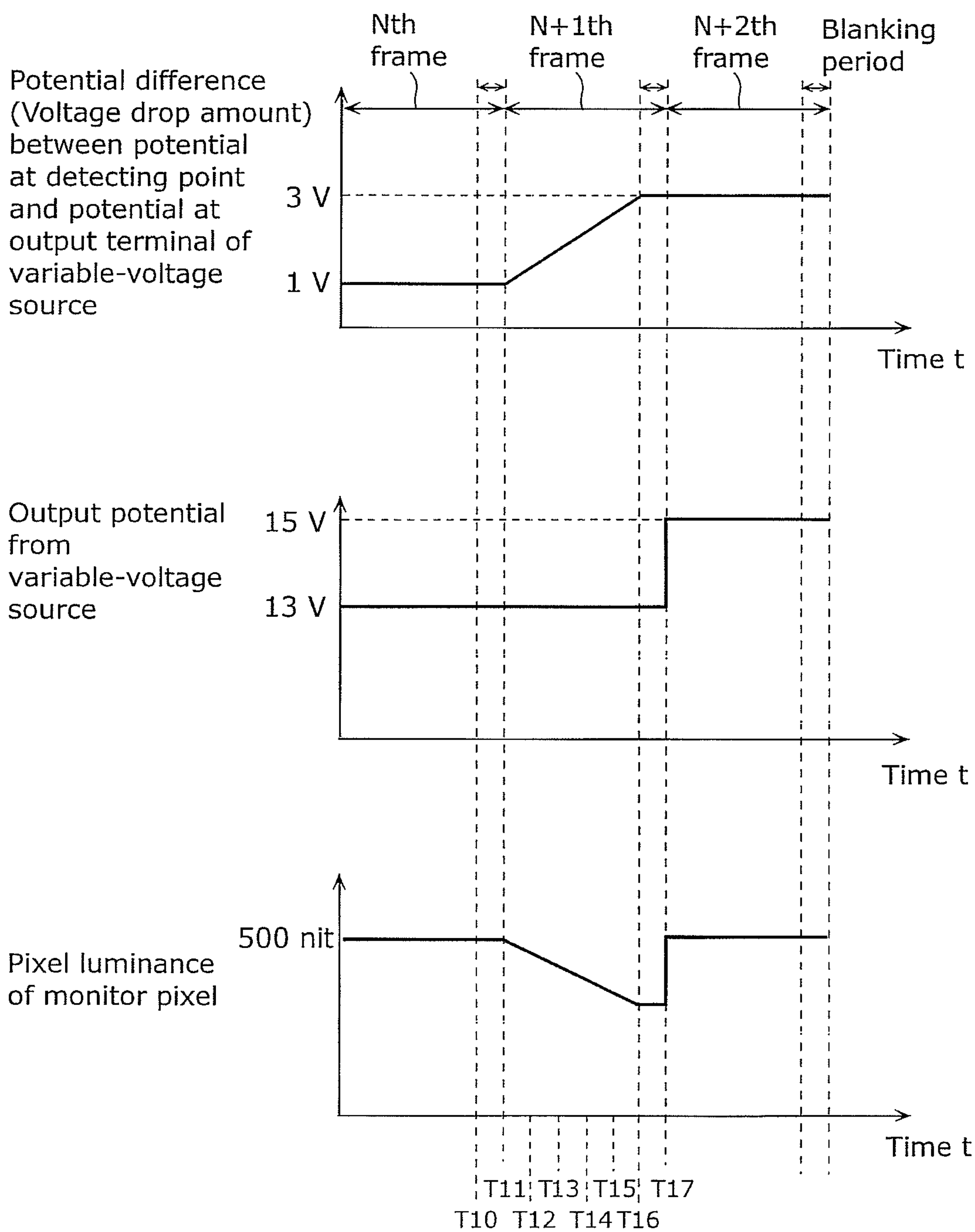

Nth frame
N+1th frame
N+2th frame
Blanking period
Potential difference (Voltage drop amount) between potential at detecting point and potential at output terminal of variable-voltage source
3 V
1 V
Time t
Output potential from variable-voltage source
15 V
13 V
Time t
Pixel luminance of monitor pixel
500 nit
Time t
T10
T11
T12
T13
T14
T15
T16
T17

FIG. 9

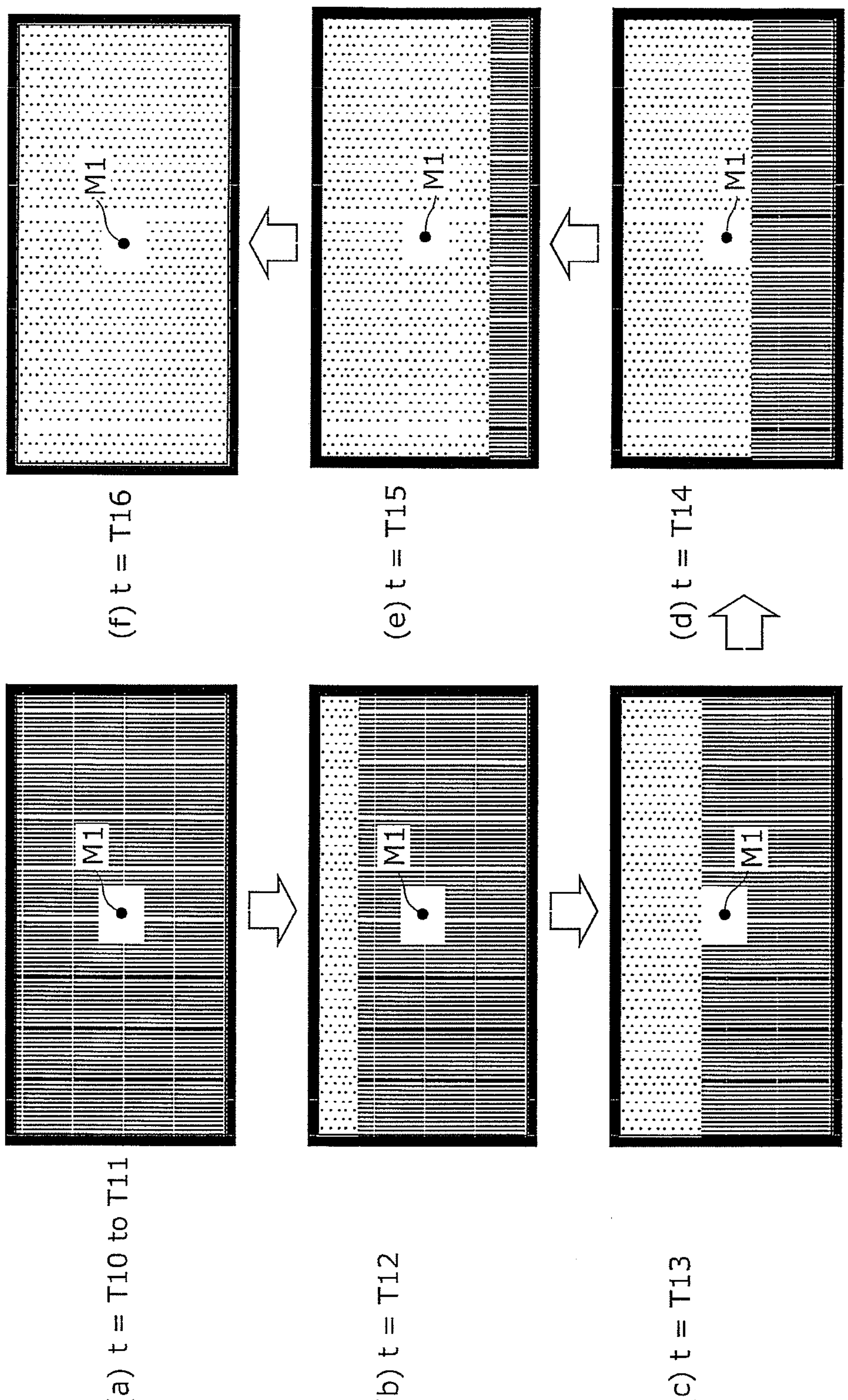


FIG. 10

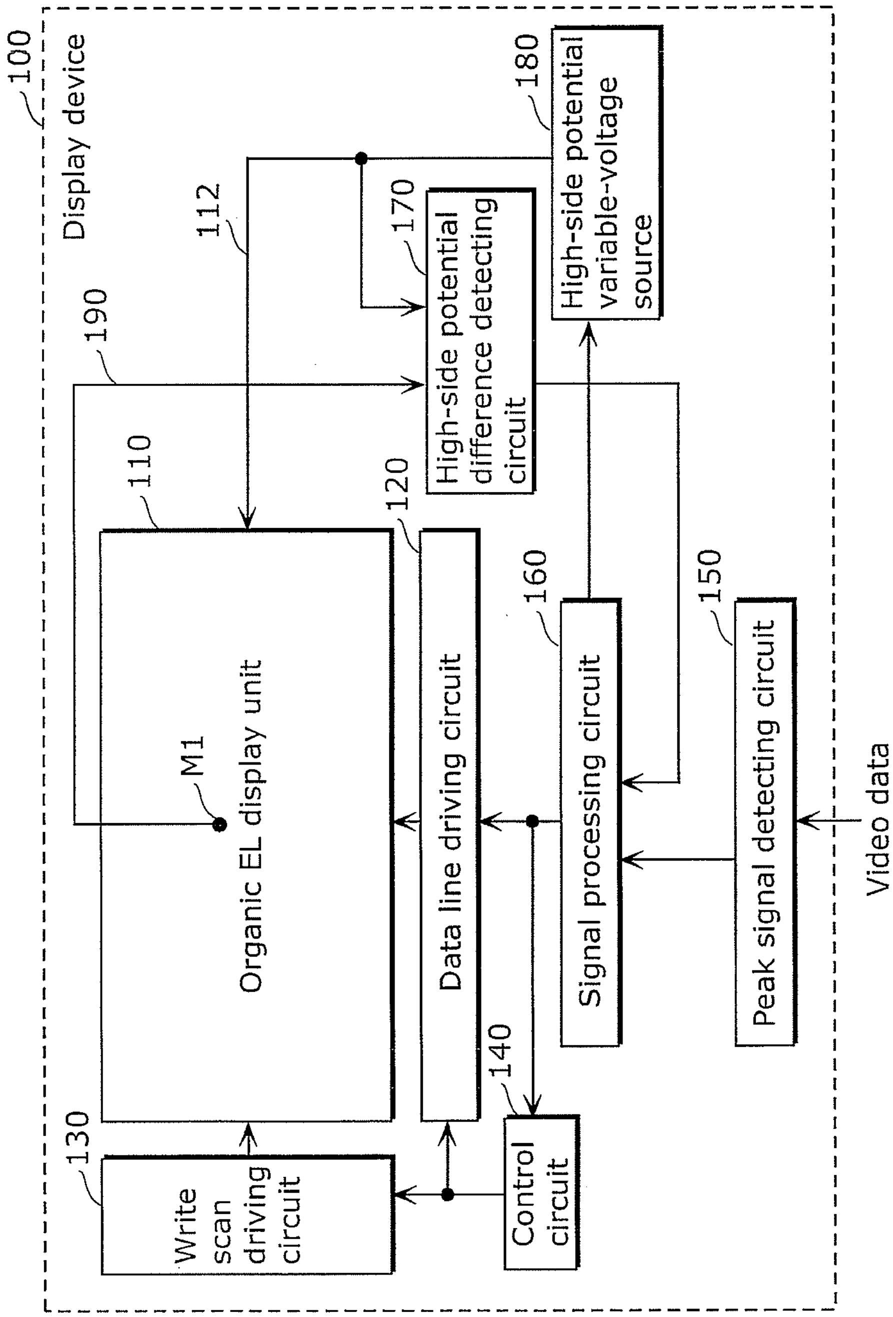

100
Display device
112
190
180
High-side potential variable-voltage source
170
High-side potential difference detecting circuit
110
Organic EL display unit
M1
120
Data line driving circuit
160
Signal processing circuit
150
Peak signal detecting circuit
Video data
140
Control circuit
130
Write scan driving circuit

FIG. 11

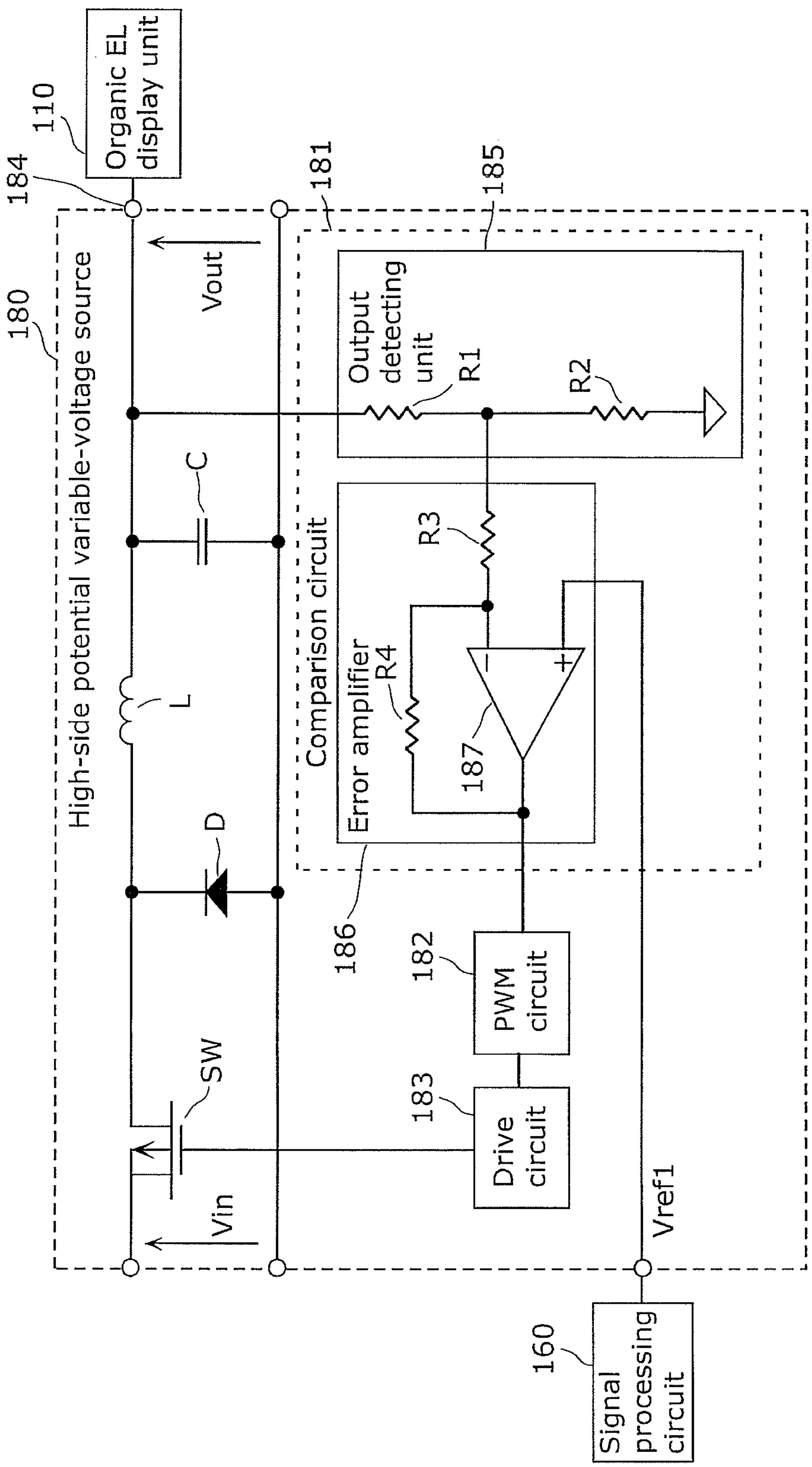

110
Organic EL display unit
184
180
High-side potential variable-voltage source
Vout
181
185
Output detecting unit
R1
R2
C
L
D
SW
Vin
Comparison circuit
Error amplifier
R3
R4
187
186
182
PWM circuit
183
Drive circuit
Vref1
160
Signal processing circuit

FIG. 12

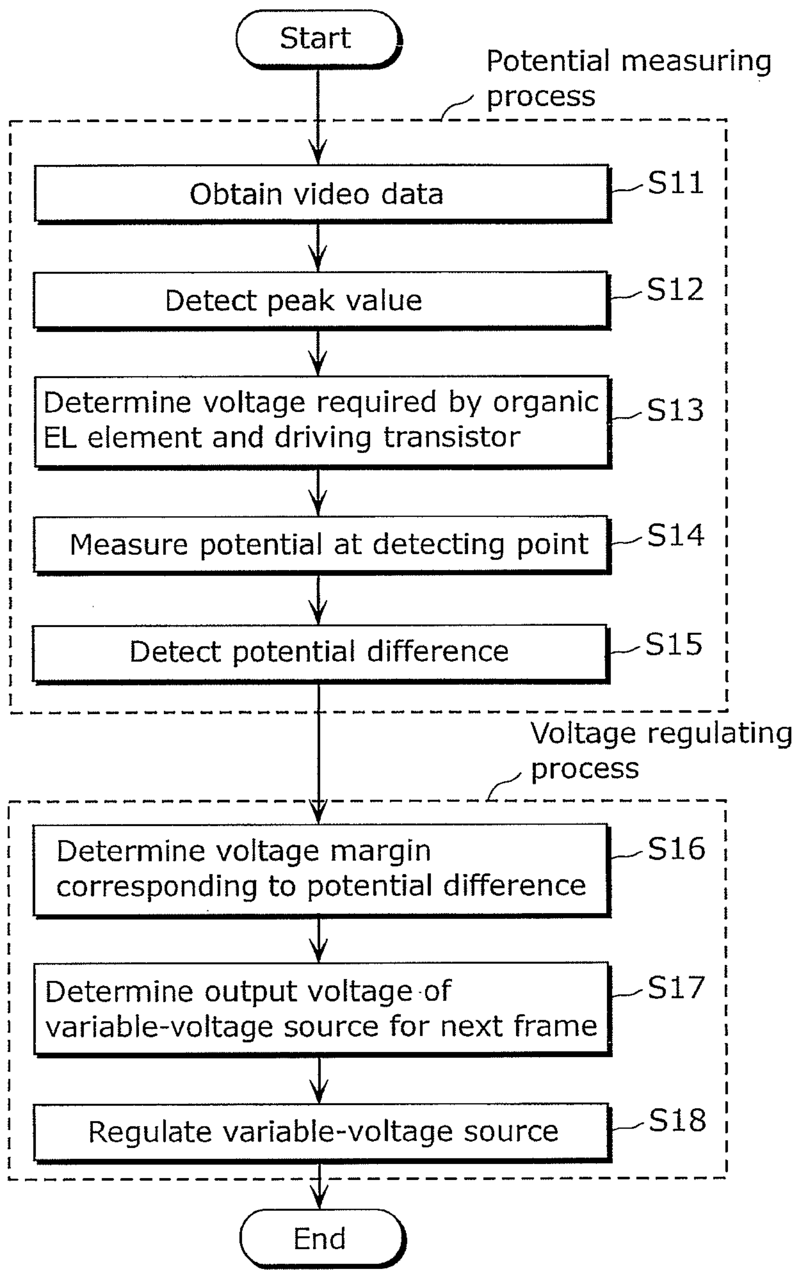

Start
Potential measuring process
Obtain video data
S11
Detect peak value
S12
Determine voltage required by organic EL element and driving transistor
S13
Measure potential at detecting point
S14
Detect potential difference
S15
Voltage regulating process
Determine voltage margin corresponding to potential difference
S16
Determine output voltage of variable-voltage source for next frame
S17
Regulate variable-voltage source
S18
End

FIG. 13

Video data (Gradation level)	Required voltage (Red)	Required voltage (Green)	Required voltage (Blue)
0	4	4.2	3.5
1	4.1	4.3	3.5
2	4.1	4.4	3.6
3	4.2	4.5	3.6
⋮	⋮	⋮	⋮
176	8.3	9.6	6.7
177	8.5	9.9	6.9
⋮	⋮	⋮	⋮
253	10.5	11.4	8.2
254	10.8	11.8	8.3
255	11.2	12.2	8.4

FIG. 14

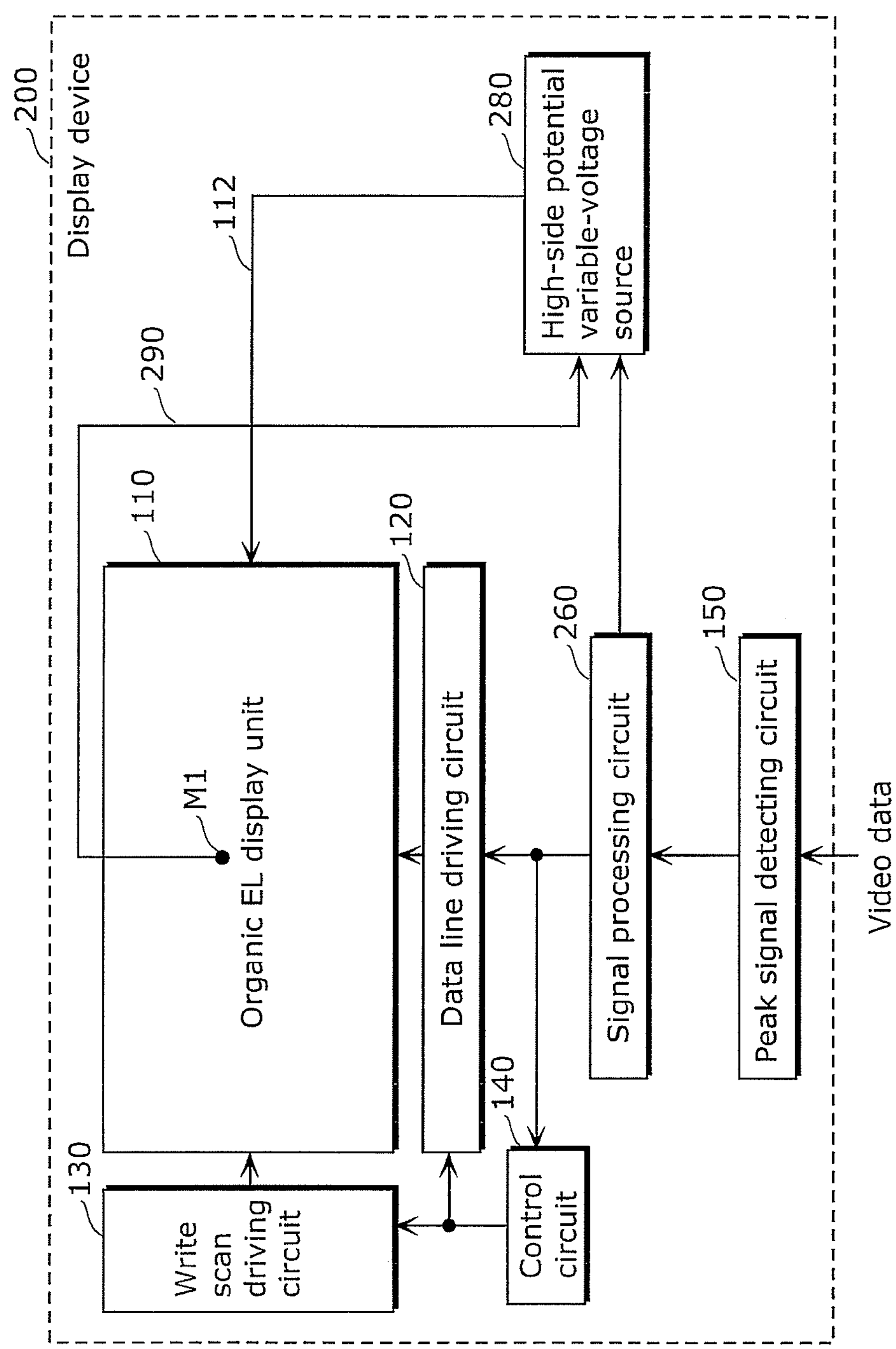

200
Display device
280
High-side potential variable-voltage source
112
290
110
Organic EL display unit
M1
120
Data line driving circuit
260
Signal processing circuit
150
Peak signal detecting circuit
Video data
140
Control circuit
130
Write scan driving circuit

FIG. 15

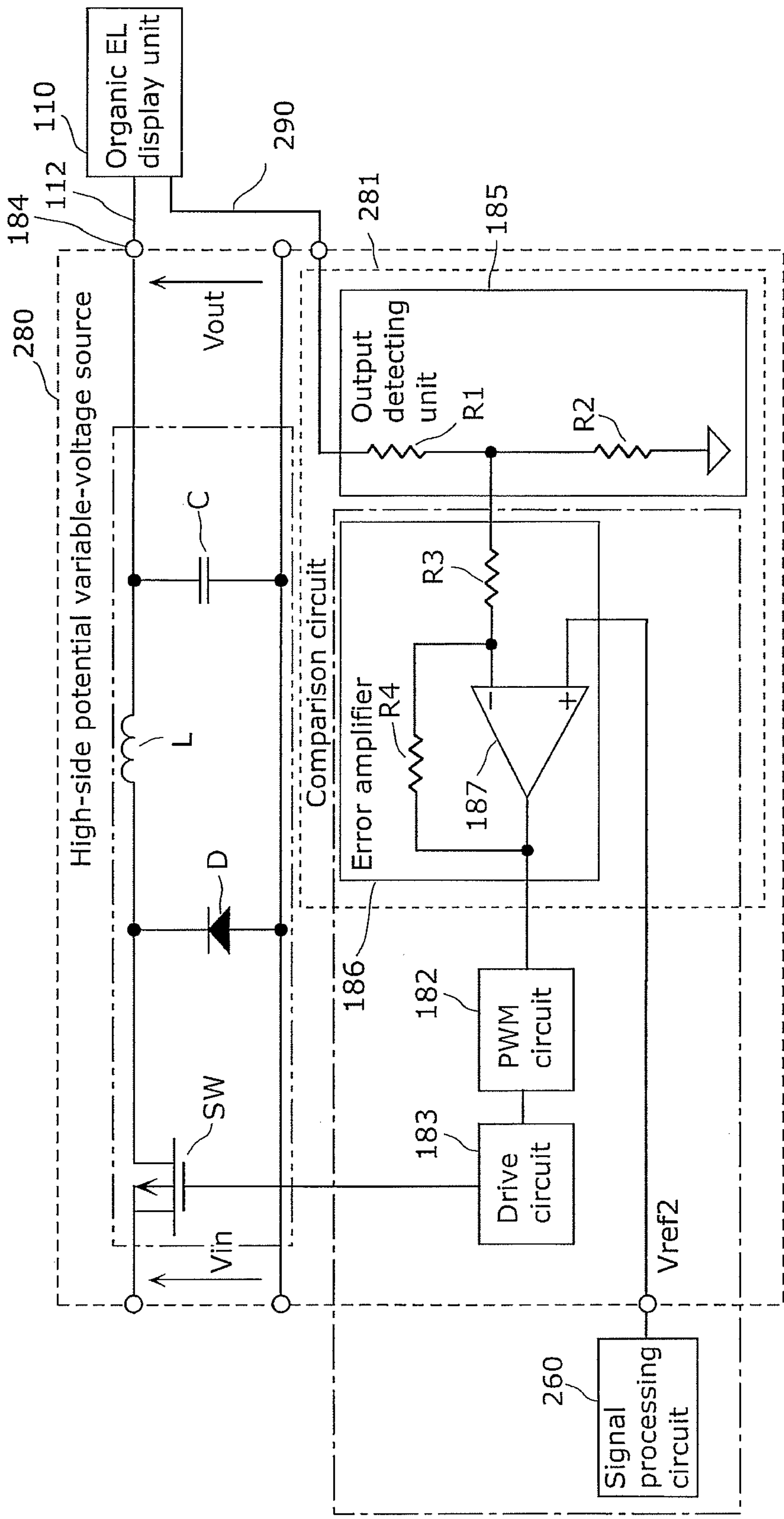
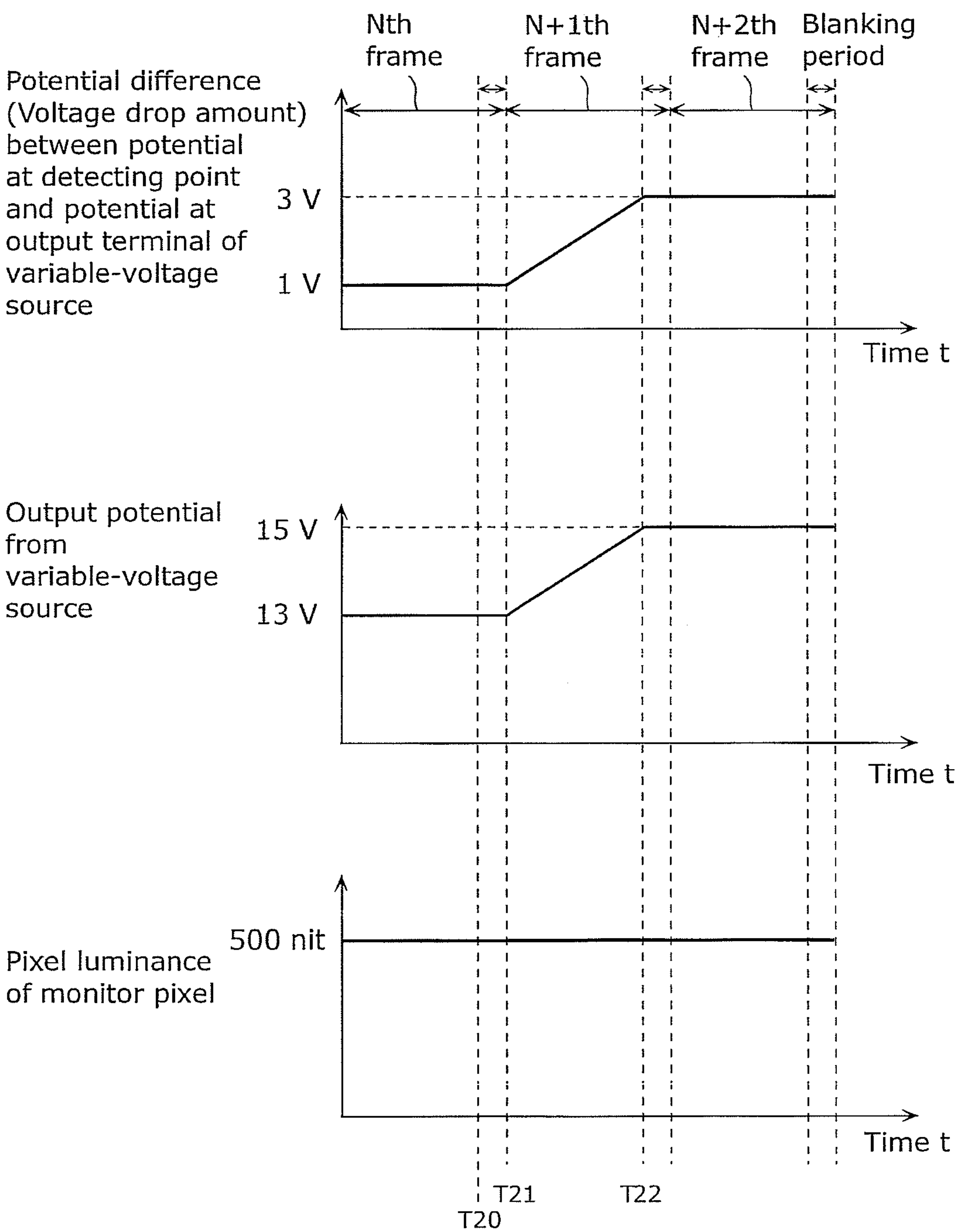

110
Organic EL display unit
112
184
290
281
185
280
High-side potential variable-voltage source
Vout
Output detecting unit
R1
R2
C
R3
Comparison circuit
Error amplifier
R4
187
L
D
186
182
PWM circuit
183
Drive circuit
SW
Vin
Vref2
260
Signal processing circuit

FIG. 16



Nth frame
N+1th frame
N+2th frame
Blanking period
Potential difference (Voltage drop amount) between potential at detecting point and potential at output terminal of variable-voltage source
3 V
1 V
Time t
Output potential from variable-voltage source
15 V
13 V
Time t
500 nit
Pixel luminance of monitor pixel
Time t
T20
T21
T22

FIG. 17

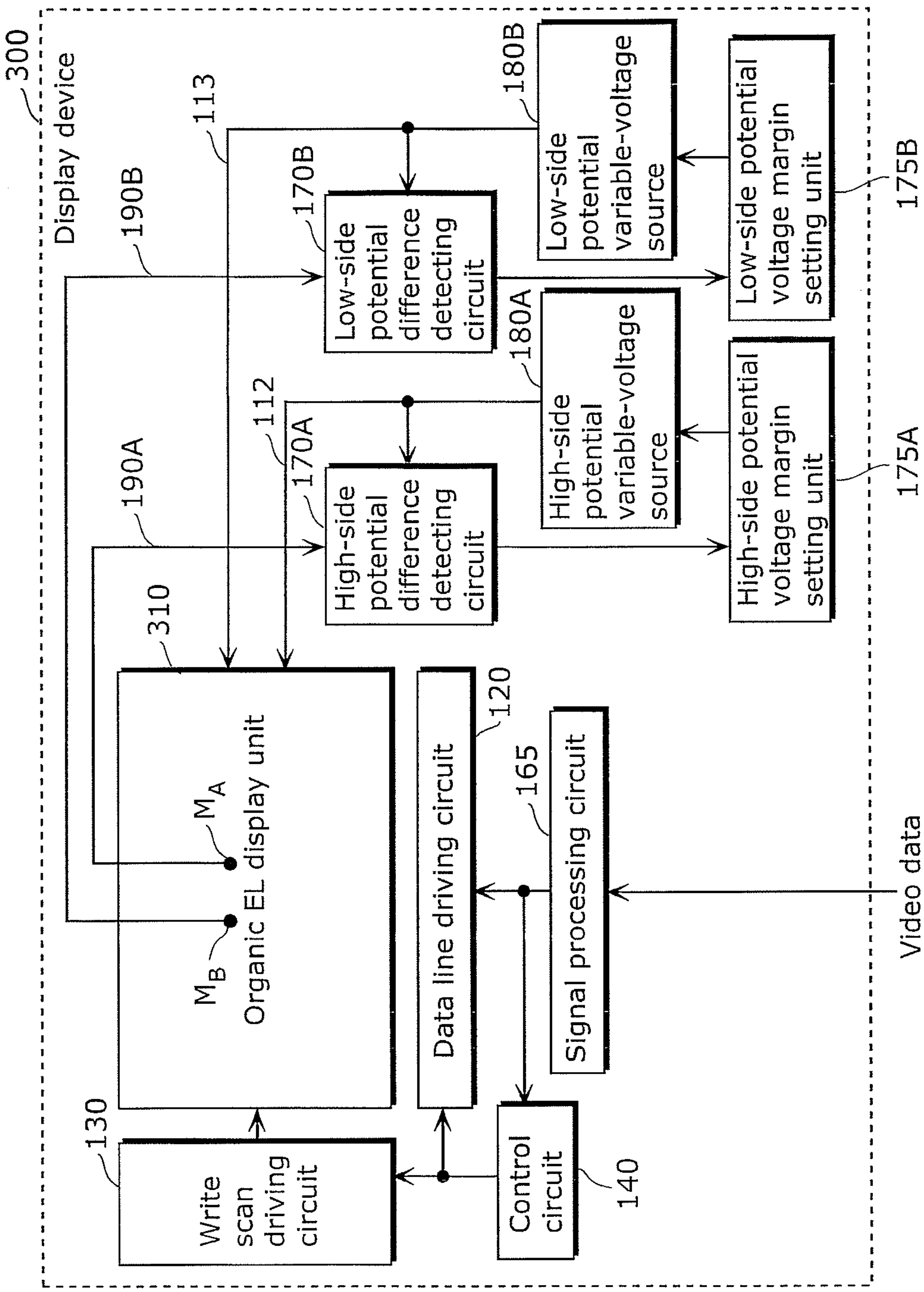

300
Display device
113
190B
180B
170B
Low-side potential variable-voltage source
Low-side potential difference detecting circuit
Low-side potential voltage margin setting unit
175B
112
190A
170A
180A
High-side potential variable-voltage source
High-side potential difference detecting circuit
High-side potential voltage margin setting unit
175A
310
M_A
M_B
Organic EL display unit
120
Data line driving circuit
165
Signal processing circuit
Video data
130
Write scan driving circuit
Control circuit
140

FIG. 18

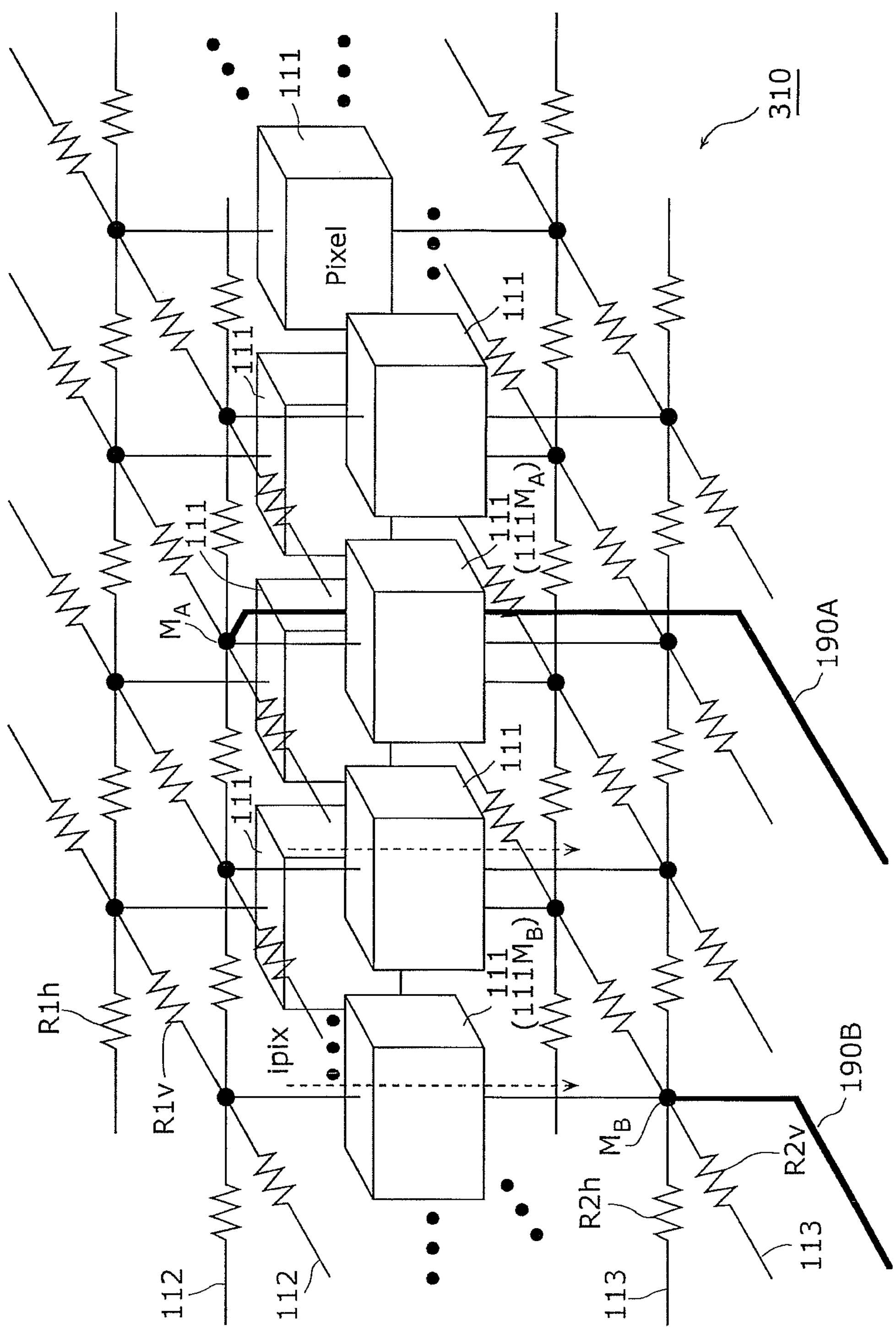

310
111
Pixel
111
111
111
111 ($111M_A$)
111
111
111
111 ($111M_B$)
M_A
M_B
190A
190B
R1h
R1v
R2h
R2v
ipix
112
112
113
113

FIG. 19A

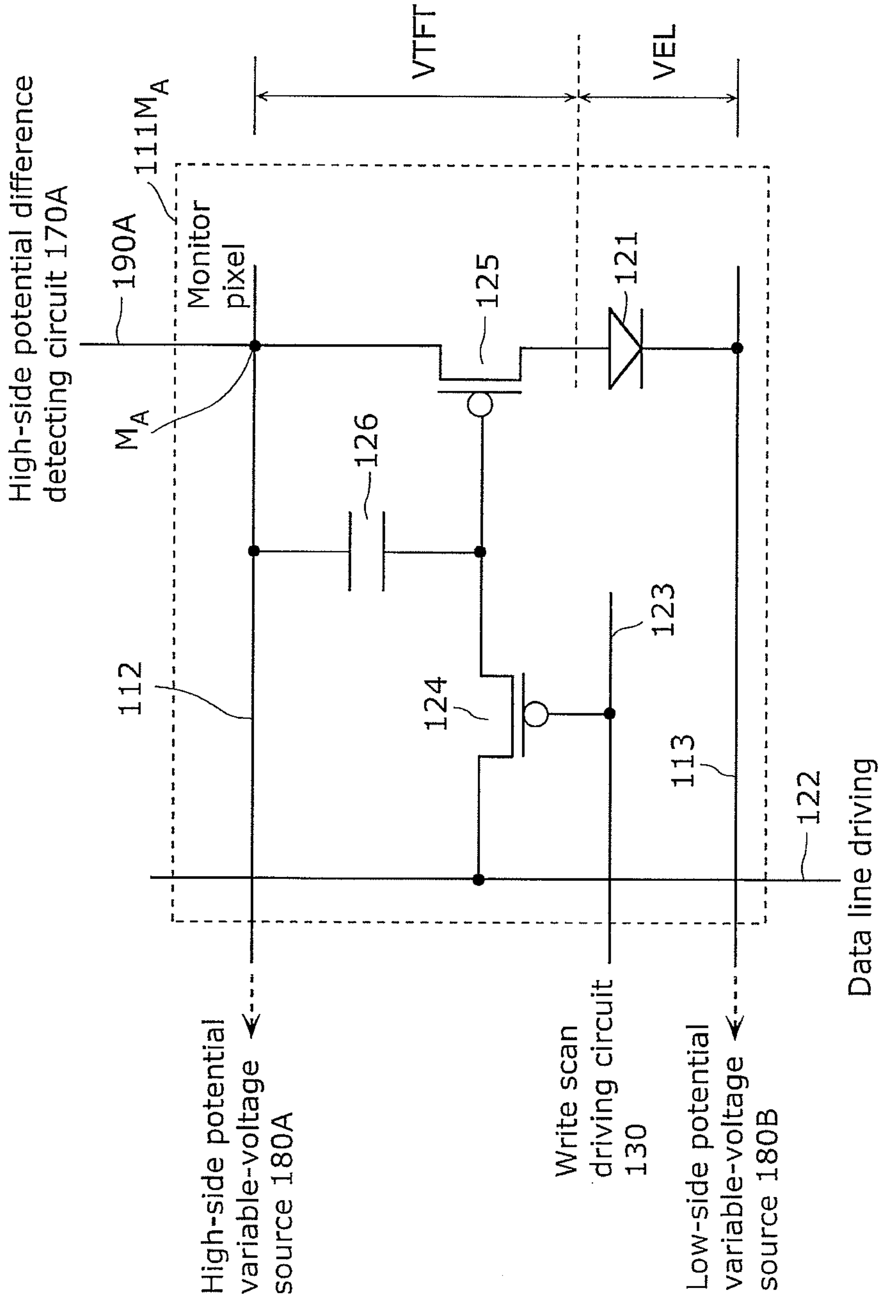

High-side potential difference detecting circuit 170A
190A
111M_A
Monitor pixel
M_A
VTFT
VEL
125
121
126
123
124
112
113
122
Data line driving circuit 120
High-side potential variable-voltage source 180A
Write scan driving circuit 130
Low-side potential variable-voltage source 180B

FIG. 19B

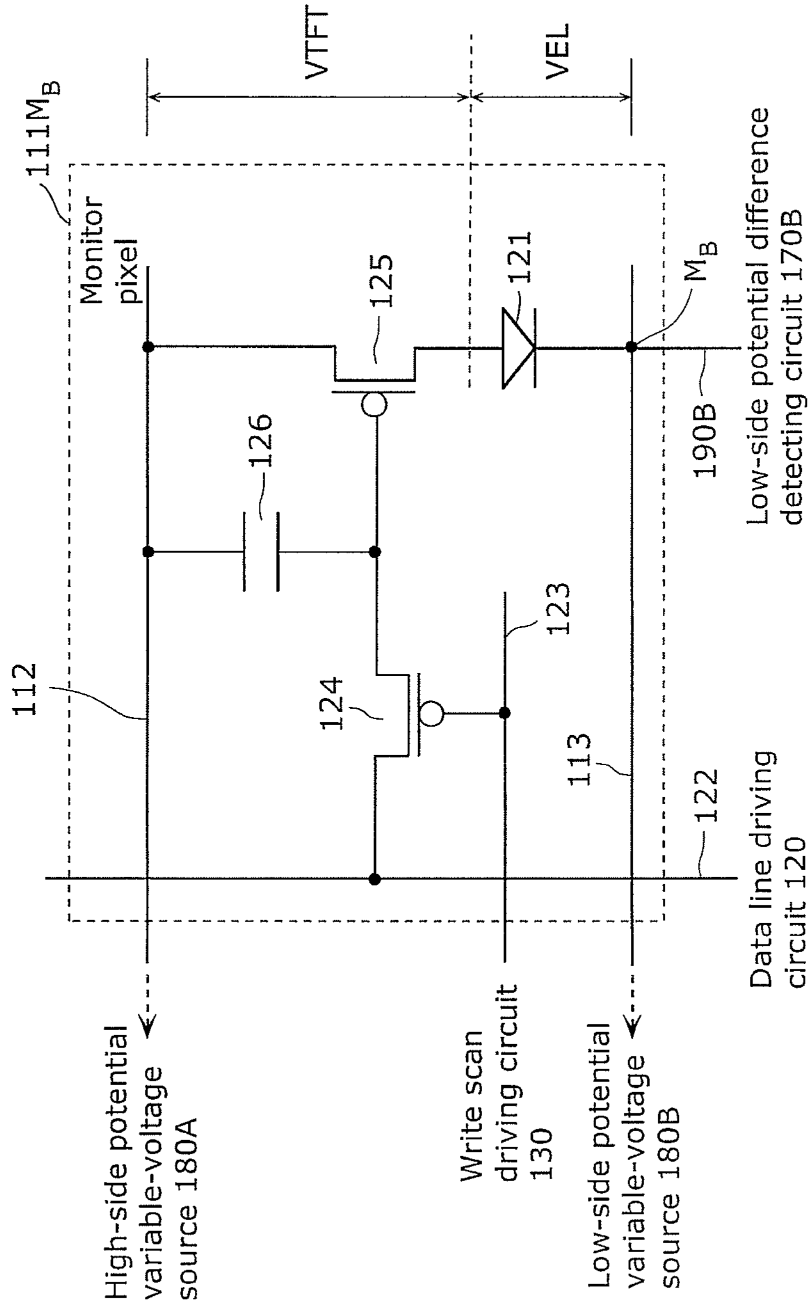

VTFT
VEL
111M_B
Monitor pixel
125
121
M_B
126
112
124
123
113
122
190B
Low-side potential difference detecting circuit 170B
Data line driving circuit 120
High-side potential variable-voltage source 180A
Write scan driving circuit 130
Low-side potential variable-voltage source 180B

FIG. 20A

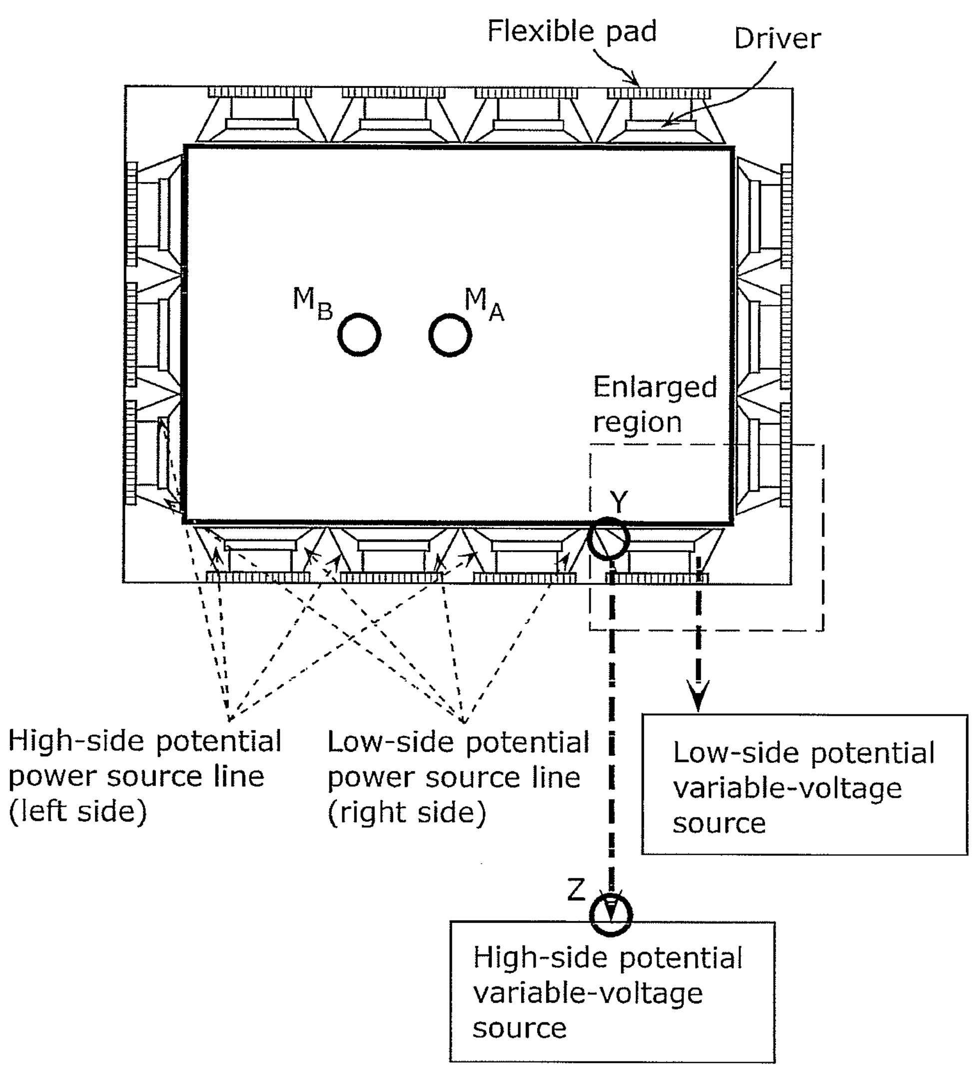

Flexible pad
Driver
M_B
M_A
Enlarged region
Y
High-side potential power source line (left side)
Low-side potential power source line (right side)
Low-side potential variable-voltage source
Z
High-side potential variable-voltage source

FIG. 20B

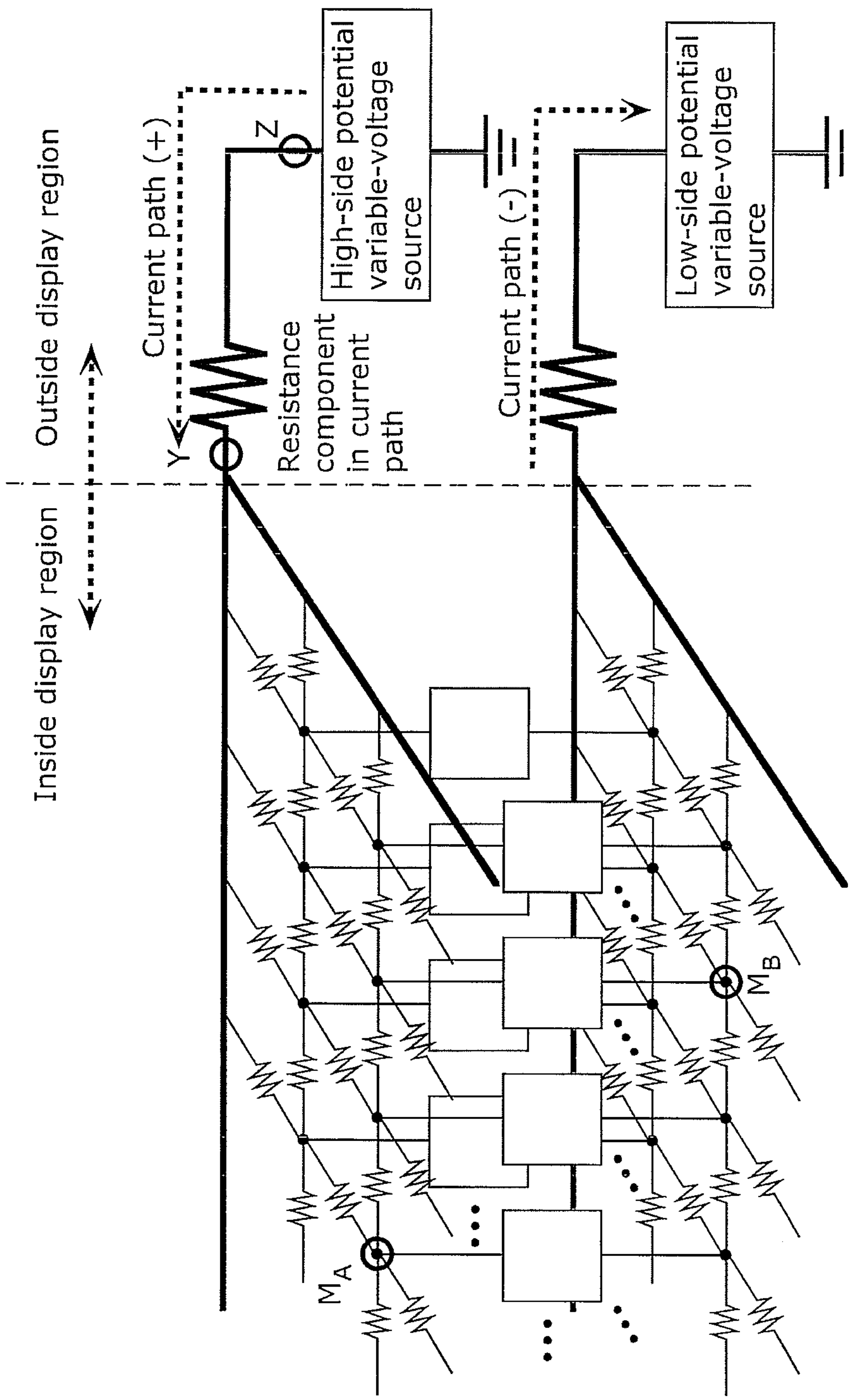

Outside display region
Inside display region
Current path (+)
Z
Y
High-side potential variable-voltage source
Resistance component in current path
Current path (-)
Low-side potential variable-voltage source
M_A
M_B

FIG. 21

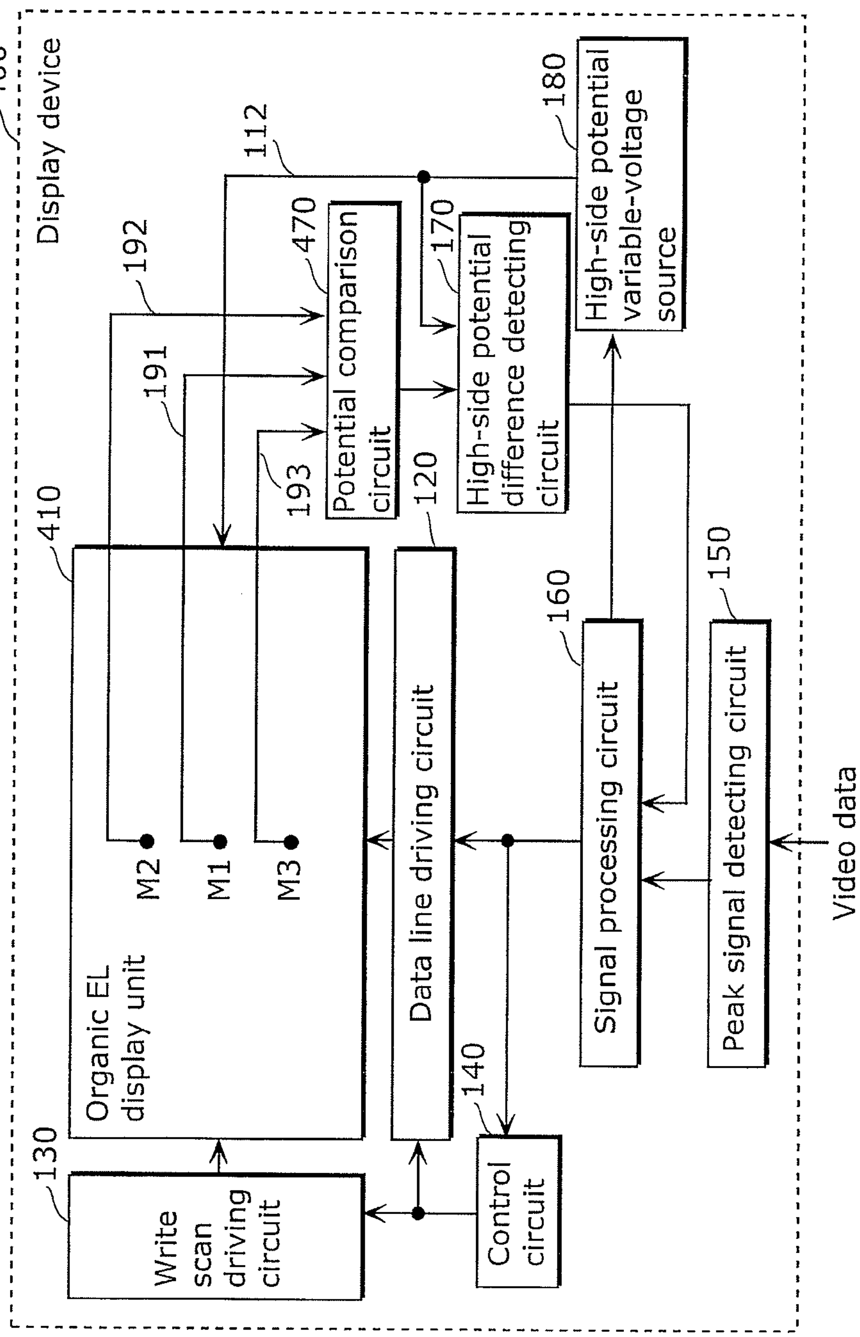

400
Display device
410
Organic EL display unit
M2
M1
M3
120
Data line driving circuit
130
Write scan driving circuit
140
Control circuit
150
Peak signal detecting circuit
160
Signal processing circuit
170
High-side potential difference detecting circuit
180
High-side potential variable-voltage source
470
Potential comparison circuit
112
191
192
193
Video data

FIG. 22

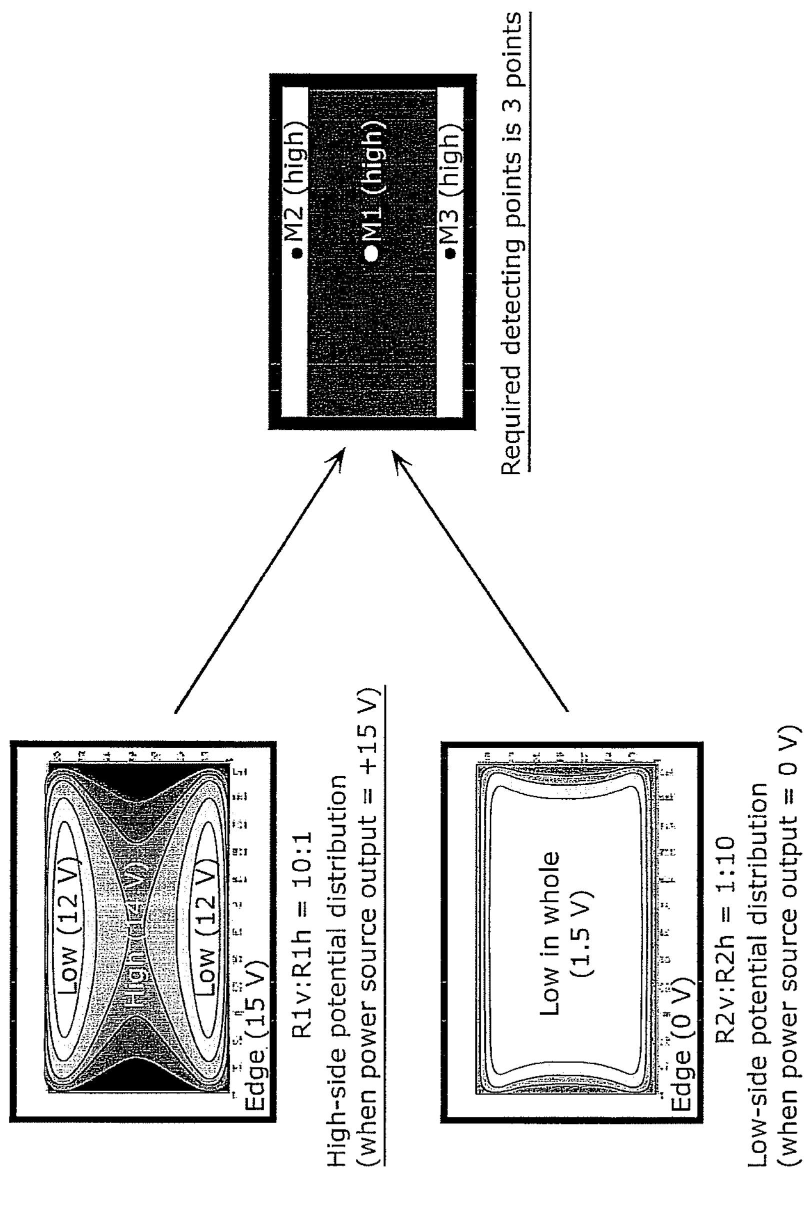

Low (12 V)
High (14 V)
Low (12 V)
Edge (15 V)
R1v:R1h = 10:1
High-side potential distribution
(when power source output = +15 V)
Low in whole
(1.5 V)
Edge (0 V)
R2v:R2h = 1:10
Low-side potential distribution
(when power source output = 0 V)
M2 (high)
M1 (high)
M3 (high)
Required detecting points is 3 points

FIG. 23

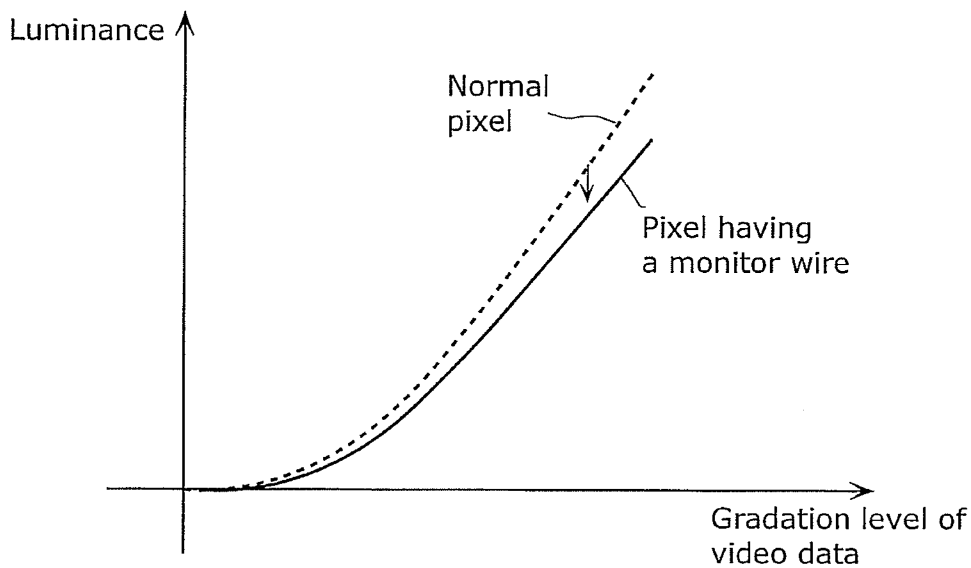

Luminance
Normal pixel
Pixel having a monitor wire
Gradation level of video data

FIG. 24

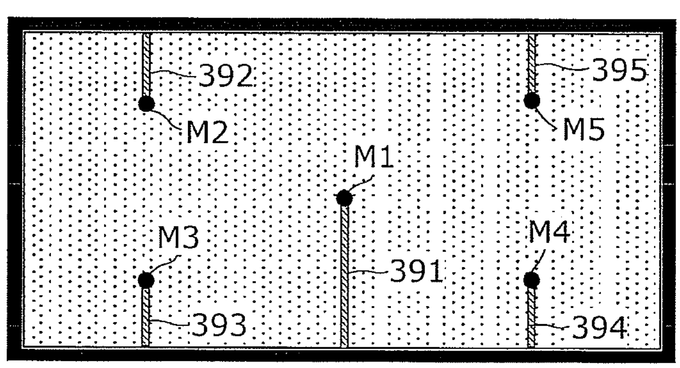
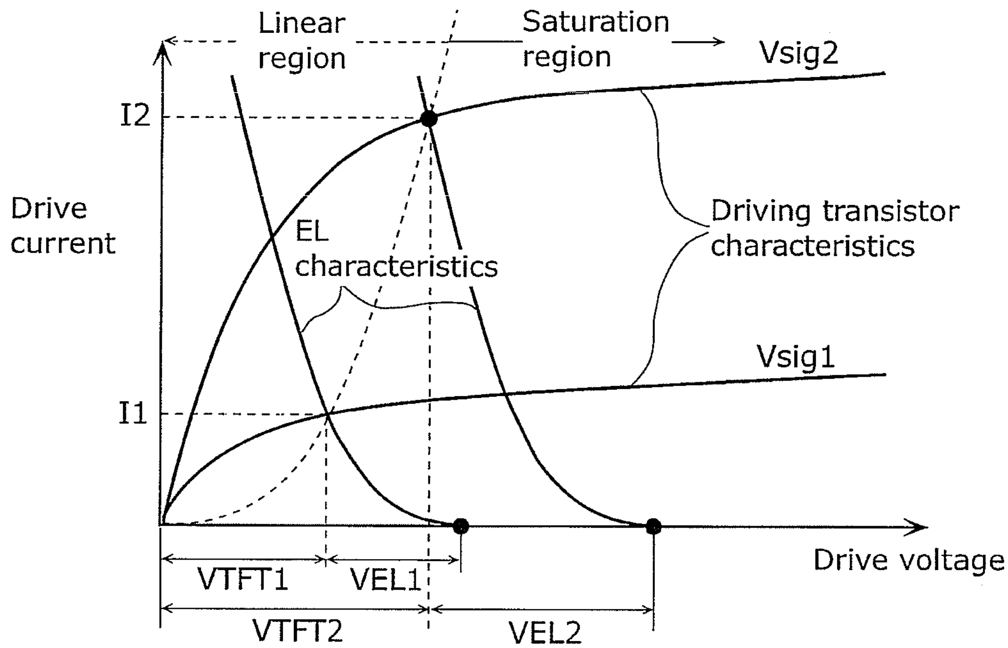
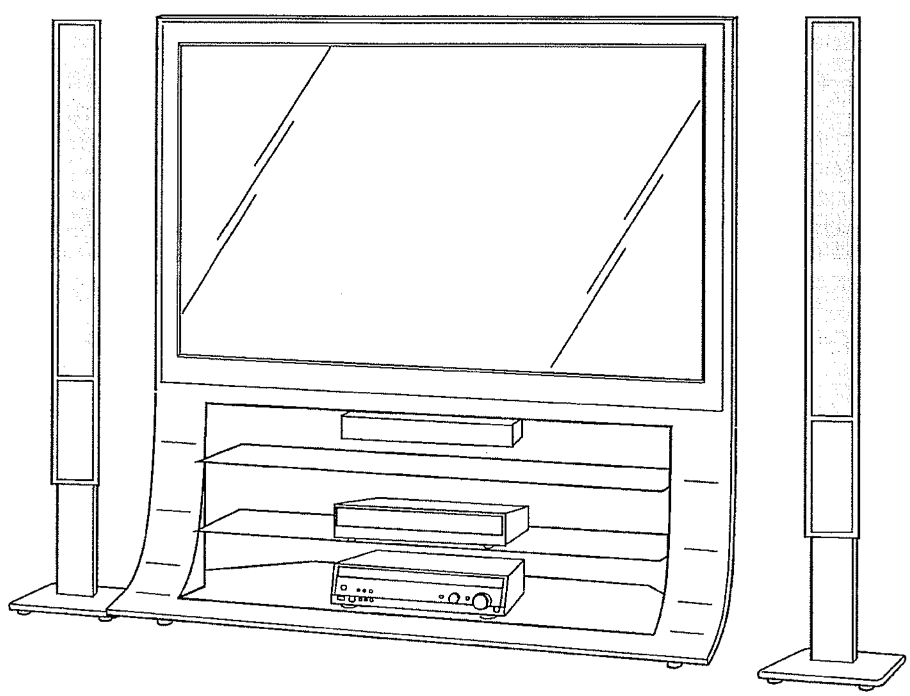

392
395
M2
M5
M1
M3
M4
391
393
394

FIG. 25



Linear region
Saturation region
Vsig2
I2
Drive current
EL characteristics
Driving transistor characteristics
Vsig1
I1
VTFT1
VEL1
Drive voltage
VTFT2
VEL2

FIG. 26



DISPLAY DEVICE

CROSS REFERENCE TO RELATED APPLICATION

This is a continuation application of PCT Patent Application No. PCT/JP2011/003424 filed on Jun. 16, 2011, designating the United States of America. The entire disclosure of the above-identified application, including the specification, drawings and claims are incorporated herein by reference in its entirety.

FIELD

One or more exemplary embodiments disclosed herein relate generally to active-matrix display devices which use current-driven luminescence elements represented by organic electroluminescence (EL) elements, and more particularly to a display device having excellent power consumption reducing effect.

BACKGROUND

In general, the luminance of an organic electroluminescence (EL) element is dependent upon the drive current supplied to the element, and the luminance of the element increases in proportion to the drive current. Therefore, the power consumption of displays made up of organic EL elements is determined by the average of display luminance. Specifically, unlike liquid crystal displays, the power consumption of organic EL displays varies significantly depending on the displayed image.

For example, in an organic EL display, the highest power consumption is required when displaying an all-white image, whereas, in the case of a typical natural image, power consumption which is approximately 20 to 40 percent of that for all-white is considered to be sufficient.

However, because power source circuit design and battery capacity entail designing which assumes the case where the power consumption of a display becomes highest, it is necessary to consider power consumption that is 3 to 4 times that for the typical natural image, and thus becoming a hindrance to the lowering of power consumption and the miniaturization of devices.

Consequently, there is conventionally proposed a technique which suppresses power consumption with practically no drop in display luminance, by detecting the peak value of video data and regulating the cathode voltage of the organic EL elements based on such detected data so as to reduce power source voltage (for example, see Patent Literature (PTL) 1).

CITATION LIST

Patent Literature

[PTL 1] Japanese Unexamined Patent Application Publication No. 2006-065148

SUMMARY

Technical Problem

Now, since an organic EL element is a current-driven element, current flows through a power source wire and a voltage drop which is proportionate to the wire resistance occurs. As such, the power supply voltage to be supplied to the display is set by adding a voltage drop margin for compensating for a voltage drop. In the same manner as the previously described power source circuit design and battery capacity, since the power drop margin for compensating for a voltage drop is set assuming the case where the power consumption of the display becomes highest, unnecessary power is consumed for typical natural images.

In a small-sized display intended for mobile device use, panel current is small and thus, compared to the voltage to be consumed by pixels, the power drop margin for compensating for a voltage drop is negligibly small. However, when current increases with the enlargement of panels, the voltage drop occurring in the power source wire no longer becomes negligible.

However, in the conventional technique in the above-mentioned Patent Reference 1, although power consumption in each of the pixels can be reduced, the power drop margin for compensating for a voltage drop cannot be reduced, and thus the power consumption reducing effect for household large-sized display devices of 30-inches and above is insufficient.

One non-limiting and exemplary embodiment provides a display device having excellent power consumption reducing effect.

Solution to Problem

In one general aspect, the techniques disclosed herein feature a display device including: a power supplying unit configured to output at least one of a high-side output potential and a low-side output potential; a display unit in which pixels are arranged and which receives power supply from the power supplying unit; a voltage detecting unit configured to detect at least one of a high-side applied potential to be applied to at least one of the pixels in the display unit and a low-side applied potential to be applied to at least one of the pixels in the display unit which is the same as or different from the at least one of the pixels to which the high-side applied potential is to be applied; and a voltage regulating unit configured to regulate at least one of the high-side output potential and the low-side output potential outputted by the power supplying unit to set, to a predetermined potential difference, a potential difference between (i) at least one of the high-side applied potential and the low-side applied potential and (ii) a reference potential.

These general and specific aspects may be implemented using a system, a method, an integrated circuit, a computer program, or a computer-readable recording medium such as a CD-ROM, or any combination of systems, methods, integrated circuits, computer programs, or computer-readable recording media.

Additional benefits and advantages of the disclosed embodiments will be apparent from the Specification and Drawings. The benefits and/or advantages may be individually obtained by the various embodiments and features of the Specification and Drawings, which need not all be provided in order to obtain one or more of such benefits and/or advantages.

Advantageous Effects

The display device according to one or more exemplary embodiments or features disclosed herein enables the implementation of a display device having excellent power consumption reducing effect.

BRIEF DESCRIPTION OF DRAWINGS

These and other advantages and features will become apparent from the following description thereof taken in conjunction with the accompanying Drawings, by way of non-limiting examples of embodiments disclosed herein.

FIG. **1** is a block diagram showing an outline configuration of a display device according to Embodiment 1 disclosed herein.

FIG. **2** is a perspective view schematically showing a configuration of an organic EL display unit according to Embodiment 1.

FIG. **3** is a circuit diagram showing an example of a specific configuration of monitor pixel.

FIG. **4** is a block diagram showing an example of a specific configuration of a high-side potential variable-voltage source according to Embodiment 1.

FIG. **5** is a flowchart showing the operation of the display device according to Embodiment 1.

FIG. **6** is a chart showing an example of a required voltage conversion table according to Embodiment 1.

FIG. **7** is a chart showing an example of a voltage margin conversion table.

FIG. **8** is a timing chart showing the operation of the display device from an Nth frame to an N+2th frame.

FIG. **9** is diagram schematically showing images displayed on the organic EL display unit.

FIG. **10** is a block diagram showing an outline configuration of a display device according to Embodiment 2 disclosed herein.

FIG. **11** is a block diagram showing an example of a specific configuration of a high-side potential variable-voltage source according to Embodiment 2.

FIG. **12** is a flowchart showing the operation of the display device according to Embodiment 2.

FIG. **13** is a chart showing an example of a required voltage conversion table according to Embodiment 2.

FIG. **14** is a block diagram showing an outline configuration of a display device according to Embodiment 3 disclosed herein.

FIG. **15** is a block diagram showing an example of a specific configuration of a high-side potential variable-voltage source according to Embodiment 3.

FIG. **16** is a timing chart showing the operation of the display device from an Nth frame to an N+2th frame.

FIG. **17** is a block diagram showing an outline configuration of a display device according to Embodiment 4 disclosed herein.

FIG. **18** is a perspective view schematically showing a configuration of an organic EL display unit according to Embodiment 4.

Claim **19**A is a diagram of the circuit configuration of a pixel connected to a high-side potential monitor wire.

FIG. **19**B is a diagram of the circuit configuration of a pixel connected to a low-side potential monitor wire.

FIG. **20**A is a diagram showing an outline configuration of a display panel included in a display device disclosed herein.

FIG. **20**B is perspective diagram schematically showing the vicinity of the periphery of the display panel included in a display device disclosed herein.

FIG. **21** is a block diagram showing an outline configuration of a display device according to Embodiment 5 disclosed herein.

FIG. **22** is a diagram showing potential distributions and a detecting point arrangement for the display device according to Embodiment 5.

FIG. **23** is a graph showing the pixel luminance of a normal pixel and the pixel luminance of a pixel having the monitor wire, which correspond to the gradation levels of video data.

FIG. **24** is a diagram schematically showing an image in which line defects occur.

FIG. **25** is a graph showing together current-voltage characteristics of the driving transistor and current-voltage characteristics of the organic EL element.

FIG. **26** is an external view of a thin flat-screen TV incorporating a display device disclosed herein.

DESCRIPTION OF EMBODIMENTS

A display device according to a general aspect of the present disclosure includes: a power supplying unit configured to output at least one of a high-side output potential and a low-side output potential; a display unit in which pixels are arranged and which receives power supply from the power supplying unit; a voltage detecting unit configured to detect at least one of a high-side applied potential to be applied to at least one of the pixels in the display unit and a low-side applied potential to be applied to at least one of the pixels in the display unit which is the same as or different from the at least one of the pixels to which the high-side applied potential is to be applied; and a voltage regulating unit configured to regulate at least one of the high-side output potential and the low-side output potential outputted by the power supplying unit to set, to a predetermined potential difference, a potential difference between (i) at least one of the high-side applied potential and the low-side applied potential and (ii) a reference potential.

Accordingly, by regulating at least one of the high-side output potential of the power supplying unit and the low-side output potential of the power supplying unit in accordance with the amount of voltage drop occurring from the power supplying unit to at least one pixel, power consumption can be reduced.

Furthermore, in the display device according to an aspect of the present disclosure, the at least one pixel for which the high-side applied potential is detected and the at least one pixel for which the low-side applied potential is detected may be different pixels.

Accordingly, when the voltage drop distribution of the high-side potential power source line and the voltage drop (rise) distribution of the low-side potential power source line are different, the output potential of the power supplying unit can be regulated based on potential information from different pixels, and thus power consumption can be reduced more effectively.

Furthermore, in the display device according to an aspect of the present disclosure, at least one of (i) the at least one pixel for which the high-side applied potential is detected and (ii) the at least one pixel for which the low-side applied potential is detected may be plural in number.

Furthermore, in a display device according to an aspect of the present disclosure, the voltage regulating unit may be configured to: select at least one applied potential from among: a lowest applied potential among high-side applied potentials detected by the voltage detecting unit; and a highest applied potential among low-side applied potentials detected by the voltage detecting unit; and regulate the power supplying unit based on the selected at least one applied potential.

Accordingly, when one of the high-side potential and the low-side potential that are detected is plural in number, it is possible to select the lowest or highest potential among the plural detected potentials. Therefore, the output potential from the power supplying unit can be more accurately regulated. Therefore, power consumption can be effectively reduced even when the size of the display unit is increased.

Furthermore, a display device according to an aspect of the present disclosure may further include at least one of: a high-side potential detecting line having one end connected to the at least one pixel for which the high-side applied potential is detected and the other end connected to the voltage detecting unit, for transmitting the high-side applied potential to the voltage detecting unit; and a low-side potential detecting line having one end connected to the at least one pixel for which the low-side applied potential is detected and the other end connected to the voltage detecting unit, for transmitting the low-side applied potential to the voltage detecting unit.

With this, the voltage detecting unit can measure at least one of (i) the high-side potential applied to the at least one pixel via the high-side potential detecting line and (ii) the low-side potential applied to at least one pixel via the low-side potential detecting line.

Furthermore, in a display device according to an aspect of the present disclosure, the voltage detecting unit may be further configured to detect at least one of the high-side output potential and the low-side output potential which are outputted by the power supplying unit, and the voltage regulating unit may be configured to regulate at least one of the high-side output potential and the low-side output potential which are outputted by the power supplying unit, in accordance with a first potential difference which is at least one of (i) a potential difference between the high-side output potential and the high-side applied potential and (ii) a potential difference between the low-side output potential and the low-side applied potential.

Accordingly, since the voltage detecting unit can actually measure the voltage drop amount from the power supplying unit up to a predetermined pixel, at least one of the high-side output potential of the power supplying unit and the low-side output potential of the power supplying unit can be set to an optimal potential that is in accordance with the voltage drop amount measured by the voltage detecting unit.

Furthermore, in a display device according to an aspect of the present disclosure, the voltage regulating unit may be configured to perform the regulation that realizes an increasing function relationship between (i) at least one of a potential difference between the high-side output potential and the reference potential and a potential difference between the low-side output potential and the reference potential and (ii) the first potential difference.

Furthermore, in a display device according to an aspect of the present disclosure, the voltage detecting unit may be further configured to detect at least one of (i) a potential in a high-side potential current path connecting the power supplying unit and a high potential side of the pixels and (ii) a potential in a low-side potential current path connecting the power supplying unit and the low potential side of the pixels; and the voltage regulating unit may be configured to regulate at least one of the high-side output potential and the low-side output potential that are outputted by the power supplying unit, in accordance with a second potential difference which is at least one of (i) a potential difference between the potential in the high-side potential current path and the high-side applied potential and (ii) a potential difference between the potential in the low-side potential current path and the low-side applied potential.

Accordingly, the output voltage from the power supplying unit can be regulated in accordance with the voltage drop amount within the display region only, by detecting the potential difference between the voltage applied to the pixels and the voltage in the wiring path outside the display region.

Furthermore, in a display device according to an aspect of the present disclosure, the voltage regulating unit may be configured to perform the regulation that realizes an increasing function relationship between (i) at least one of a potential difference between the high-side output potential and the reference potential and a potential difference between the low-side output potential and the reference potential and (ii) the second potential difference.

Furthermore, in a display device according to an aspect of the present disclosure, each of the pixels may include: a driving element having a source electrode and a drain electrode; and a luminescence element having a first electrode and a second electrode, the first electrode being connected to one of the source electrode and the drain electrode of the driving element, the high-side applied potential may be applied to one of the second electrode and the other of the source electrode and the drain electrode, and the low-side applied potential may be applied to the other of the second electrode and the other of the source electrode and the drain electrode.

Furthermore, in a display device according to an aspect of the present disclosure, the pixels may be arranged in rows and columns, the display device may further include a first power source line and a second power source line, the first power source line connecting the others of the source electrode and the drain electrode of the respective driving elements of adjacent pixels in at least one of the row direction and the column direction, and the second power source line connecting the second electrodes of the respective luminescence elements of adjacent pixels in the row direction and the column direction, and the pixels may receive the power supply from the power supplying unit via the first power source line and the second power source line.

Furthermore, in a display device according to an aspect of the present disclosure, the second electrode and the second power source line may be part of a common electrode that is common to the pixels, and may be electrically connected to the power supplying unit so that a potential is applied to the common electrode from a periphery of the common electrode.

Accordingly, although the voltage drop amount becomes larger towards the vicinity of the center of the display unit, the high-side output potential of the power supplying unit and the low-side output potential of the power supplying unit can be appropriately regulated and thus power consumption can be further reduced, particularly when the size of the display unit is increased.

Furthermore, in a display device according to an aspect of the present disclosure, the second electrode may comprise a transparent conductive material including a metal oxide.

Furthermore, in a display device according to an aspect of the present disclosure, the luminescence element may be an organic electroluminescence (EL) element.

Accordingly, since heat generation can be suppressed through the reduction of power consumption, the deterioration of the organic EL element can be suppressed.

These general and specific aspects may be implemented using a system, a method, an integrated circuit, a computer program, or a computer-readable recording medium such as a CD-ROM, or any combination of systems, methods, integrated circuits, computer programs, or computer-readable recording media.

Hereinafter, certain exemplary embodiments are described in greater detail with reference to the accompanying Drawings. It is to be noted that, in all the figures, the same reference numerals are given to the same or corresponding elements and redundant description thereof shall be omitted.

Each of the exemplary embodiments described below shows a general or specific example. The numerical values, shapes, materials, structural elements, the arrangement and connection of the structural elements, steps, the processing order of the steps etc. shown in the following exemplary embodiments are mere examples, and therefore do not limit the scope of the appended Claims and their equivalents. Therefore, among the structural elements in the following exemplary embodiments, structural elements not recited in any one of the independent claims are described as arbitrary structural elements.

Embodiment 1

A display device according to this embodiment includes: a variable-voltage source which outputs at least one of a high-side output potential and a low-side output potential; an organic electroluminescence (EL) display unit in which pixels are arranged and which receives power supply from the variable-voltage source; a potential difference detecting circuit which detects at least one of a high-side applied potential to be applied to one pixel in the organic EL display unit and a low-side applied potential to be applied to at least one pixel that is the same or different from the one pixel; and a signal processing circuit which regulates at least one of the high-side output potential and the low-side output potential outputted from the variable-voltage source to set, to a predetermined potential difference, a potential difference between (i) at least one of the high-side applied potential and the low-side applied potential to be applied to the pixels and (ii) a reference potential.

Accordingly, the display device according to this embodiment realizes excellent power consumption reducing effect.

Hereinafter, Embodiment 1 shall be specifically described with reference to the Drawings.

FIG. **1** is a block diagram showing an outline configuration of the display device according to Embodiment 1.

A display device **50** shown in the figure includes an organic electroluminescence (EL) display unit **110**, a data line driving circuit **120**, a write scan driving circuit **130**, a control circuit **140**, a signal processing circuit **165**, a high-side potential difference detecting circuit **170**, a voltage margin setting unit **175**, a high-side potential variable-voltage source **180**, and a monitor wire **190**.

FIG. **2** is a perspective view schematically showing a configuration of the organic EL display unit **110** according to Embodiment 1. It is to be noted that the lower portion of the figure is the display screen side.

As shown in the figure, the organic EL display unit **110** includes the pixels **111**, the first power source wire **112**, and the second power source wire **113**.

Each pixel **111** is connected to the first power source wire **112** and the second power source wire **113**, and produces luminescence at a luminance that is in accordance with a pixel current ipix that flows to the pixel **111**. At least one predetermined pixel out of the pixels **111** is connected to the monitor wire **190** at a high-side potential detecting point M1. Hereinafter, the pixel **111** that is directly connected to the monitor wire **190** shall be denoted as monitor pixel **111**M.

The first power source wire **112** is arranged in a net-like manner to correspond to pixels **111** that are arranged in a matrix, and is electrically connected to the high-side potential variable-voltage source **180** disposed at the periphery of the organic EL display unit **110**. Through the outputting of a high-side power source potential from the high-side potential variable-voltage source **180**, a potential corresponding to the high-side power source potential outputted by the high-side potential variable-voltage source **180** is applied to the first power source wire **112**. On the other hand, the second power source wire **113** is formed in the form of a continuous film on the organic EL display unit **110**. In FIG. **2**, the first power source wire **112** and the second power source wire **113** are schematically illustrated in mesh-form in order to show the resistance components of the first power source wire **112** and the second power source wire **113**. It is to be noted that the second power source wire **113** may be grounded to, for example, a common grounding potential of the display device **50**, at the periphery of the organic EL display unit **110**.

A horizontal first power source wire resistance R1*h* and a vertical first power source wire resistance R1*v* are present in the first power source wire **112**. A horizontal second power source wire resistance R2*h* and a vertical second power source wire resistance R2*v* are present in the second power source wire **113**. It is to be noted that, although not illustrated, each of the pixels **111** is connected to the write scan driving circuit **130** and the data line driving circuit **120**, and is also connected to a scanning line for controlling the timing at which the pixel produces luminescence and stops producing luminescence, and to a data line for supplying signal voltage corresponding to the pixel luminance of the pixel **111**.

The optimal position of the monitor pixel **111**M is determined depending on the wiring method of the first power source wire **112**, and the respective values of the first power source wire resistances R1*h* and R1*v*.

FIG. **3** is a circuit diagram showing an example of a specific configuration of the monitor pixel **111**M. Each of the pixels arranged in a matrix includes a driving element and a luminescence element. The driving element includes a source electrode and a drain electrode. The luminescence element includes a first electrode and a second electrode. The first electrode is connected to one of the source electrode and the drain electrode of the driving element. The high-side potential is applied to one of (i) the other of the source electrode and the drain electrode and (ii) the second electrode, and the low-side potential is applied to the other of (i) the other of the source electrode and the drain electrode and (ii) the second electrode.

Specifically, each of the pixels **111** includes an organic EL element **121**, a data line **122**, a scanning line **123**, a switch transistor **124**, a driving transistor **125**, and a holding capacitor **126**. Furthermore, in the monitor pixel **111**M, the monitor wire **190**A is additionally connected to the other of the source electrode and the drain electrode of the driving element. At least one pixel **111**M is disposed in the organic EL display unit **110**.

The organic EL element **121** is a luminescence element having an anode electrode, which is a first electrode, connected to the drain electrode of the driving transistor **125** and a cathode electrode, which is a second electrode, connected to the second power source wire **113**, and produces luminescence with a luminance that is in accordance with the pixel current ipix flowing between the anode electrode and the cathode electrode. The cathode electrode of the organic EL element **121** forms part of a common electrode provided in common to the plural pixels **111**, and potential is applied to the common electrode from the periphery of the common electrode. Specifically, the common electrode functions as the second power source wire **113** in the organic EL display unit **110**. Furthermore, the cathode electrode is formed from a transparent conductive material made of a metallic oxide.

The data line **122** is connected to the data line driving circuit **120** and one of the source electrode and the drain electrode of the switch transistor **124**, and signal voltage corresponding to video data is applied to the data line **122** by the data line driving circuit **120**.

The scanning line **123** is connected to the write scan driving circuit **130** and the gate electrode of the switch transistor **124**, and switches between conduction and non-conduction of the switching transistor **124** according to the voltage applied by the write scan driving circuit **130**.

The switching transistor **124** has one of a source electrode and a drain electrode connected to the data line **122**, the other of the source electrode and the drain electrode connected to the gate electrode of the driving transistor **125** and one end of the holding capacitor **126**, and is, for example, a P-type thin-film transistor (TFT).

The driving transistor **125** is a driving element having a source electrode connected to first power source wire **112**, a drain electrode connected to the anode electrode of the organic EL element **121**, and a gate electrode connected to the one end of the holding capacitor **126** and the other of the source electrode and the drain electrode of the switching transistor **124**, and is, for example, a P-type TFT. With this, the driving transistor **125** supplies the organic EL element **121** with current that is in accordance with the voltage held in the holding capacitor **126**. Furthermore, in the monitor pixel **111**M, the source of the driving transistor **125** is connected to the monitor wire **190**.

The holding capacitor **126** has one end connected to the other of the source electrode and the drain electrode of the switch transistor **124**, and the other end connected to the first power source wire **112**, and holds the potential difference between the potential of the first power source wire **112** and the potential of the gate electrode of the driving transistor **125** when the switch transistor **124** becomes non-conductive. Specifically, the holding capacitor **126** holds a voltage corresponding to the signal voltage.

The functions of the respective constituent elements shown in FIG. **1** shall be described below with reference to FIG. **2** and FIG. **3**.

The data line driving circuit **120** outputs signal voltage corresponding to video data, to the pixels **111** via the data lines **122**.

The write scan driving circuit **130** sequentially scans the pixels **111** by outputting a scanning signal to scanning lines **123**. Specifically, the switch transistors **124** are switched between conduction and non-conduction on a per row basis. With this, the signal voltages outputted to the data lines **122** are applied to the pixels **111** in the row selected by the write scan driving circuit **130**. Therefore, the pixels **111** produce luminescence with a luminance that is in accordance with the video data.

The control circuit **140** instructs the drive timing to each of the data line driving circuit **120** and the write scan driving circuit **130**.

The signal processing circuit **165** outputs, to the data line driving circuit **120**, a signal voltage corresponding to inputted video data.

The high-side potential difference detecting circuit **170**, which is the voltage detecting unit in this embodiment, measures, for the monitor pixel **111**M, the high-side potential to be applied to the monitor pixel **111**M. Specifically, the high-side potential difference detecting circuit **170** measures, via the monitor wire **190**, the high-side potential to be applied to the monitor pixel **111**M. Specifically, the high-side potential difference detecting circuit **170** measures the potential at the detecting point M**1**. In addition, the high-side potential difference detecting circuit **170** measures the output potential of the high-side potential variable-voltage source **180**, and measures the potential difference ΔV between the measured high-side potential to be applied to the monitor pixel **111**M and the output potential of the high-side potential variable-voltage source **180**. Subsequently, the high-side potential difference detecting circuit **170** outputs the measured potential difference ΔV to the voltage margin setting unit **175**.

The voltage margin setting unit **175**, which is the voltage regulating unit in this embodiment, regulates, based on a voltage (VEL+VTFT) at a peak gradation level and the potential difference ΔV detected by the high-side potential difference detecting circuit **170**, the high-side potential variable-voltage source **180** to set the potential difference between the potential of the monitor pixel **111**M and the reference potential to a predetermined voltage. Specifically, the voltage margin setting unit **175** calculates a voltage drop margin Vdrop, based on the potential difference detected by the high-side potential difference detecting circuit **170**. Subsequently, the voltage margin setting unit **175** sums up the voltage (VEL+VTFT) at the peak gradation level and the voltage drop margin Vdrop, and outputs the summation result VEL+VTFT+Vdrop, as the voltage of a first reference voltage Vref**1**A, to the high-side potential variable-voltage source **180**.

The high-side potential variable-voltage source **180**, which is the power supplying unit in this embodiment, outputs the high-side potential to the organic EL display unit **110**. The high-side potential variable-voltage source **180** outputs an output voltage Vout for setting the potential difference between the high-side potential of the monitor pixel **111**M and the reference potential to the predetermined voltage (VEL+VTFT), according to the first reference voltage Vref**1**A outputted by the voltage margin setting unit **175**. It is sufficient that reference potential be a potential serving as a reference in the display device **50**, and is for example a ground potential in this embodiment.

The monitor wire **190** is a high-side potential detecting line which has one end connected to the monitor pixel **111**M and the other end connected to the high-side potential difference detecting circuit **170**, and transmits the high-side potential applied to the monitor pixel **111**M to the high-side potential difference detecting circuit **170**.

Next, a brief description of the detailed configuration of the high-side potential variable-voltage source **180** shall be given.

FIG. **4** is a block diagram showing an example of a specific configuration of a high-side potential variable-voltage source according to Embodiment 1. It is to be noted that the organic EL display unit **110** and the voltage margin setting unit **175** which are connected to the variable-voltage source are also shown in the figure.

The high-side potential variable-voltage source **180** shown in the figure includes a comparison circuit **181**, a pulse width modulation (PWM) circuit **182**, a drive circuit **183**, a switching element SW, a diode D, an inductor L, a capacitor C, and an output terminal **184**, and converts an input voltage Vin into an output voltage Vout which is in accordance with the first reference voltage Vref**1**, and outputs the output voltage Vout from the output terminal **184**. It is to be noted that, although not illustrated, an AC-DC converter is provided in a stage ahead of an input terminal to which the input voltage Vin is inputted, and it is assumed that conversion, for example, from 100V AC to 20V DC is already carried out.

The comparison circuit **181** includes an output detecting unit **185** and an error amplifier **186**, and outputs a voltage that is in accordance with the difference between the output voltage Vout and the first reference voltage Vref**1**A, to the PWM circuit **182**.

The output detecting unit **185**, which includes two resistors R**1** and R**2** provided between the output terminal **184** and a grounding potential, voltage-divides the output voltage Vout in accordance with the resistance ratio between the resistors R**1** and R**2**, and outputs the voltage-divided output voltage Vout to the error amplifier **186**.

The error amplifier **186** compares the Vout that has been voltage-divided by the output detection unit **185** and the first reference voltage Vref**1**A outputted by the voltage margin setting unit **175**, and outputs, to the PWM circuit **182**, a voltage that is in accordance with the comparison result. Specifically, the error amplifier **186** includes an operational amplifier **187** and resistors R**3** and R**4**. The operational amplifier **187** has an inverting input terminal connected to the output detecting unit **185** via the resistor R**3**, a non-inverting input terminal connected to the voltage margin setting unit **175**, and an output terminal connected to the PWM circuit **182**. Furthermore, the output terminal of the operational amplifier **187** is connected to the inverting input terminal via the resistor R**4**. With this, the error amplifier **186** outputs, to the PWM circuit **182**, a voltage that is in accordance with the potential difference between the voltage inputted from the output detecting unit **185** and the first reference voltage Vref**1**A inputted from the voltage margin setting unit **175**. Stated differently, the error amplifier **186** outputs, to the PWM circuit **182**, a voltage that is in accordance with the potential difference between the output voltage Vout and the first reference voltage Vref**1**A.

The PWM circuit **182** outputs, to the drive circuit **183**, pulse waveforms having different duties depending on the voltage outputted by the comparison circuit **181**. Specifically, the PWM circuit **182** outputs a pulse waveform having a long ON duty when the voltage outputted by the comparison circuit **181** is large, and outputs a pulse waveform having a short ON duty when the outputted voltage is small. Stated differently, the PWM circuit **182** outputs a pulse waveform having a long ON duty when the potential difference between the output voltage Vout and the first reference voltage Vref**1**A is big, and outputs a pulse waveform having a short ON duty when the potential difference between the output voltage Vout and the first reference voltage Vref**1**A is small. It is to be noted that the ON period of a pulse waveform is a period in which the pulse waveform is active.

The drive circuit **183** turns ON the switch SW during the period in which the pulse waveform outputted by the PWM circuit **182** is active, and turns OFF the switch SW during the period in which the pulse waveform outputted by the PWM circuit **182** is inactive.

The switching element SW is switched between conduction and non-conduction by the drive circuit **183**. The input voltage Vin is outputted, as the output voltage Vout, to the output terminal **184** via the inductor L and the capacitor C only while the switching element is in the state of conduction. Accordingly, from 0V, the output voltage Vout gradually approaches 20V (Vin). At this time the inductor L and the capacitor C are charged. Since voltage is applied (charged) to both ends of the inductor L, the output voltage Vout becomes a potential which is lower than the input voltage Vin by such voltage.

As the output voltage Vout approaches the first reference voltage Vref**1**A, the voltage inputted to the PWM circuit **182** becomes smaller, and the ON duty of the pulse signal outputted by the PWM circuit **182** becomes shorter.

Then, the time in which the switching element SW is ON also becomes shorter, and the output voltage Vout gently converges with the first reference voltage Vref**1**A.

The potential of the output voltage Vout, while having slight voltage fluctuations, eventually settles to a potential in the vicinity of Vout=Vref**1**A.

In this manner, the high-side potential variable-voltage source **180** generates the output voltage Vout which becomes the first reference voltage Vref**1**A outputted by the signal processing circuit **165**, and supplies the output voltage Vout to the organic EL display unit **110**.

Next, the operation of the aforementioned display device **50** shall be described using FIG. **5** to FIG. **7**.

FIG. **5** is a flowchart showing the operation of the display device **50** according to Embodiment 1.

First, the voltage margin setting unit **175** reads, from a memory, the preset voltage (VEL+VTFT) corresponding to the peak gradation level (step S**10**). Specifically, voltage margin setting unit **175** determines the VTFT+VEL corresponding to the gradation levels for each color, using a required voltage conversion table indicating the required voltage VTFT+VEL corresponding to the gradation levels for each color.

FIG. **6** is a chart showing an example of a required voltage conversion table which is referenced by the voltage margin setting unit **175**. As shown in the figure, required voltages VTFT+VEL respectively corresponding to the peak gradation level (gradation level **255**) are stored in the required voltage conversion table. For example, the required voltage at the peak gradation level of R is 11.2 V, the required voltage at the peak gradation level of G is 12.2 V, and the required voltage at the peak gradation level of B is 8.4 V. Among the required voltages at the peak gradation levels of the respective colors, the largest voltage is the 12.2 V of G. Therefore, the voltage margin setting unit **175** determines VTFT+VEL to be 12.2 V.

Meanwhile, the high-side potential difference detecting circuit **170** detects the potential at the detecting point M**1** via the monitor wire **190** (step S**14**).

Next, the high-side potential difference detecting circuit **170** receives the voltage of the output terminal **184** of the high-side potential variable-voltage source **180**, calculates the potential difference between potential at the detecting point M**1** and the reference potential, and detects the potential difference ΔV between the received potential of the output terminal **184** and the calculated potential difference (step S**15**). Subsequently, the high-side potential difference detecting circuit **170** outputs the detected potential difference ΔV to the voltage margin setting unit **175**. It is to be noted that the steps S**10** to S**15** up to this point correspond to the potential measuring process according to the present disclosure.

Next, the voltage margin setting unit **175** determines a voltage drop margin Vdrop corresponding to the potential difference ΔV detected by the high-side potential difference detecting circuit **170**, based on a potential difference signal outputted by the high-side potential difference detecting circuit **170** (step S**16**). Specifically, the voltage margin setting unit **175** has a voltage margin conversion table indicating the voltage drop margin Vdrop corresponding to the potential difference ΔV, and determines the voltage drop margin Vdrop with reference to the conversion table.

FIG. **7** is a chart showing an example of the voltage margin conversion table that is referenced by the voltage margin setting unit **175**.

As shown in the figure, voltage drop margins Vdrop respectively corresponding to the potential differences ΔV are stored in the voltage margin conversion table. For example, when the potential difference ΔV is 3.4 V, the voltage drop margin Vdrop is 3.4 V. Therefore, the voltage margin setting unit **175** determines the voltage drop margin Vdrop to be 3.4 V.

Now, as shown in the voltage margin conversion table, the potential difference ΔV and the voltage drop margin Vdrop have an increasing function relationship. Furthermore, the output voltage Vout of the high-side potential variable-voltage source **180** rises with a bigger voltage drop margin Vdrop. In other words, the potential difference ΔV and the output voltage Vout have an increasing function relationship.

Next, the voltage margin setting unit **175** determines the output voltage Vout that the high-side potential variable-voltage source **180** is to be made to output in the next frame period (step S**17**). Specifically, the output voltage Vout that the high-side potential variable-voltage source **180** is to be made to output in the next frame period is assumed to be VTFT+VEL+Vdrop which is the sum value of (i) VTFT+VEL determined in the determination (step S**13**) of the voltage required by the organic EL element **121** and the driving transistor **125** and (ii) the voltage drop margin Vdrop determined in the determination (step S**15**) of the voltage margin corresponding to the potential difference ΔV.

Lastly, the voltage margin setting unit **175** regulates the high-side potential variable-voltage source **180** by setting the first reference voltage Vref**1**A as VTFT+VEL+Vdrop at the beginning of the next frame period (step S**18**). With this, in the next frame period, the high-side potential variable-voltage source **180** supplies Vout=VTFT+VEL+Vdrop to the organic EL display unit **110**. It is to be noted that step S**16** to step S**18** correspond to the voltage regulating process according to the present disclosure.

In this manner, the display device **50** according to this embodiment includes: the high-side potential variable-voltage source **180** which outputs the high-side potential; the high-side potential difference detecting circuit **170** which measures, for the monitor pixel **111**M in the organic EL display unit **110**, (i) the high-side potential applied to the monitor pixel **111**M and (ii) the high-side potential output voltage Vout of the high-side potential variable-voltage source **180**; and the voltage margin setting unit **175** which regulates the high-side potential variable-voltage source **180** to set, to the predetermined potential (VTFT+VEL), the potential difference between the reference potential and the high-side potential that is applied to the monitor pixel **111**M that is measured by the high-side potential difference detecting circuit **170**. Furthermore, the high-side potential difference detecting circuit **170**, in addition, measures the high-side potential output voltage Vout of the high-side potential variable-voltage source **180**, detects the potential difference between the measured high-side potential output voltage Vout and the high-side potential applied to the monitor pixel **111**M. The voltage margin setting unit **175** regulates the high-side potential variable-voltage source **180** in accordance with the potential difference detected by the high-side potential difference detecting circuit **170**.

With this, the display device **50** can reduce excess voltage and reduce power consumption by detecting the voltage drop caused by the horizontal first power source wire resistance R**1***h* and a vertical first power source wire resistance R**1***v* and giving feedback to the high-side potential variable-voltage source **180** regarding the degree of such voltage drop.

Furthermore, in the display device **50**, the monitor pixel **111**M is located near the center of the organic EL display unit **110**, and thus the output voltage Vout of the high-side potential variable-voltage source **180** can be easily regulated even when the size of the organic EL display unit **110** is increased.

Furthermore, since heat generation by the organic EL element **121** is suppressed through the reduction of power consumption, the deterioration of the organic EL element **121** can be prevented.

Next, the display pattern transition in the case where the video data inputted up to the Nth frame changes from the N+1th frame onward, in the display device **50** described above, shall be described using FIG. **8** and FIG. **9**.

Initially, the video data that is assumed to have been inputted in the Nth frame and the N+1th frame shall be described.

First, it is assumed that, up to the Nth frame, the video data corresponding to the central part of the organic EL display unit **110** is a peak gradation level (R:G:B=255:255:255) in which the central part of the organic EL display unit **110** is seen as being white. On the other hand, it is assumed that the video data corresponding to a part of the organic EL display unit **110** other than the central part is a gray gradation level (R:G:B=50:50:50) in which the part of the organic EL display unit **110** other than the central part is seen as being gray.

Furthermore, from the N+1th frame onward, it is assumed that the video data corresponding to the central part of the organic EL display unit **110** is the peak gradation level (R:G:B=255:255:255) as in the Nth frame. On the other hand, it is assumed that the video data corresponding to the part of the organic EL display unit **110** other than the central part is a gray gradation level (R:G:B=150:150:150) that can be seen as a brighter gray than in the Nth frame.

Next, the operation of the display device **50** in the case where video data as described above is inputted in the Nth frame and the N+1th frame shall be described.

FIG. **8** is a timing chart showing the operation of the display device **50** from the Nth frame to the N+2th frame.

The potential difference ΔV detected by the high-side potential difference detecting circuit **170**, the output voltage Vout from the high-side potential variable-voltage source **180**, and the pixel luminance of the monitor pixel **111**M are shown in the figure. Furthermore, a blanking period is provided at the end of each frame period.

FIG. **9** is diagram schematically showing images displayed on the organic EL display unit.

In a t=T**10**, the signal processing circuit **165** receives input of the video data of the Nth frame. The voltage margin setting unit **175** uses the required voltage conversion table and sets the 12.2 V required voltage at the peak gradation level of G to the voltage (VTFT+VEL).

Meanwhile, at this time, the high-side potential difference detecting circuit **170** detects the potential at the detecting point M**1** via the monitor wire **190**, and detects the potential difference ΔV between the detected potential and the output voltage Vout outputted from the high-side potential variable-voltage source **180**. For example, in time t=T**10**, the high-side potential difference detecting circuit **170** detects ΔV=1V. Subsequently, the voltage margin setting unit **175** uses the voltage margin conversion table and determines the voltage drop margin Vdrop for the N+1th frame to be 1 V.

A time t=T**10** to T**11** is the blanking period of the Nth frame. In this period, an image which is the same as that in the time t=T**10** is displayed in the organic EL display unit **110**.

(a) in FIG. **9** schematically shows an image displayed on the organic EL display unit **110** in the time t=T**10** to T**11**. In this period, the image displayed on the organic EL display unit **110** corresponds to the image data of the Nth frame, and thus the central part is white and the part other than the central part is gray.

In time t=T**11**, the voltage margin setting unit **175** sets the voltage of the first reference voltage Vref**1**A as the sum VTFT+VEL+Vdrop (for example, 13.2 V) of the aforementioned voltage (VTFT+VEL) and the voltage drop margin Vdrop.

Over a time t=T**11** to T**16**, the image corresponding to the video data of the N+1th frame is gradually displayed on the organic EL display unit **110** ((b) to (f) in FIG. **9**). At this time, the output voltage Vout from the high-side potential variable-voltage source **180** is, at all times, the VTFT+VEL+Vdrop set to the voltage of the first reference voltage Vref**1**A in time t=T**11**. However, the video data corresponding to the part of the organic EL display unit **110** other than the central part is a gray gradation level that can be seen as a gray that is brighter than that in the Nth frame. Therefore, the amount of current supplied by the high-side potential variable-voltage source

180 to the organic EL display unit **110** gradually increases over time t=T**11** to T**16**, and the voltage drop in the first power source wire **112** gradually increases following this increase in the amount of current. With this, there is a shortage of power source voltage for the pixels **111** in the central part of the organic EL display unit **110**, which are the pixels **111** in a brightly displayed region. Stated differently, luminance drops below the image corresponding to the video data R:G:B=255:255:255 of the N+1th frame. Specifically, over the time t=T**11** to T**16**, the pixel luminance of the pixels **111** at the central part of the organic EL display unit **110** gradually drops.

In a time t=T**16**, the signal processing circuit **165** receives input of the video data of the N+1th frame. The voltage margin setting unit **175** uses the required voltage conversion table and continues to set the 12.2 V required voltage at the peak gradation level of G to the voltage (VTFT+VEL).

Meanwhile, at this time, the high-side potential difference detecting circuit **170** detects the potential at the detecting point M**1** via the monitor wire **190**, and detects the potential difference ΔV between (i) the potential difference between the detected potential at the detecting point M**1** and the reference potential and (ii) and the output voltage Vout outputted from the high-side potential variable-voltage source **180**. For example, in time t=T**16**, the high-side potential difference detecting circuit **170** detects ΔV=3 V. Subsequently, the voltage margin setting unit **175** uses the voltage margin conversion table and determines the voltage drop margin Vdrop for the N+1th frame to be 3 V.

Next, in time t=T**17**, the voltage margin setting unit **175** sets the voltage of the first reference voltage Vref**1**A to the sum VTFT+VEL+Vdrop (for example, 15.2 V) of the aforementioned voltage (VTFT+VEL) and the voltage drop margin Vdrop. Therefore, from time t=T**17** onward, the potential at the detecting point M**1** becomes VTFT+VEL which is the predetermined potential.

In this manner, in the display device **100**, although luminance temporarily drops in the N+1th frame, this is a very short period and thus has practically no impact on the user.

It is to be noted that although, in this embodiment, the high-side potential applied to the pixel **111**M is monitored and the high-side potential outputted from the high-side potential variable-voltage source **180** is regulated to set the potential difference between the monitored high-side potential and the reference potential to a predetermined voltage, the low-side potential applied to the pixel **111**M may be monitored and the low-side potential outputted from a low-side potential variable-voltage source may be regulated to set the potential difference between the monitored low-side potential and the reference potential to a predetermined voltage. In this case, a low-side potential difference detecting circuit is provided in place of the high-side potential difference detecting circuit **170** shown in FIG. **1**, and a low-side potential variable-voltage source is provided in place of the high-side potential variable-voltage source **180**.

The function of the voltage margin setting unit is the same as that of the voltage margin setting unit **175**. The voltage margin setting unit regulates, based on a voltage (VEL+VTFT) at a peak gradation level and the potential difference ΔV detected by the low-side potential difference detecting circuit, the low-side potential variable-voltage source to set the potential of the monitor pixel **111**M to a predetermined potential.

The low-side potential difference detecting circuit measures, for the monitor pixel **111**M, a low-side potential applied to the monitor pixel **111**M. In addition, the low-side potential difference detecting circuit measures the output potential of the low-side potential variable-voltage source, and measures the potential difference ΔV between (i) the potential difference between the measured low-side potential applied to the monitor pixel **111**M and the reference potential and (ii) the output potential of the low-side variable-voltage source. Subsequently, the low-side potential difference detecting circuit outputs the measured potential difference ΔV to the voltage margin setting unit.

The low-side potential variable-voltage source outputs the low-side potential to the organic EL display unit **110**. The low-side potential variable-voltage source outputs an output voltage Vout for setting the potential difference between the low-side potential of the monitor pixel **111**M and the reference potential to a predetermined potential, according to a reference voltage Vref outputted by the voltage margin setting unit. It is sufficient that reference potential be a potential serving as a reference in the display device **50**.

With this, the display device in the present disclosure can reduce excess voltage and reduce power consumption by detecting the voltage drop caused by the horizontal second power source wire resistance R**2***h* and the vertical second power source wire resistance R**2***v* and giving feedback to the low-side potential variable-voltage source regarding the degree of such voltage drop.

Furthermore, since heat generation by the organic EL element is suppressed through the reduction of power consumption, the deterioration of the organic EL element can be prevented.

Embodiment 2

Compared to the display device according to Embodiment 1, a display device according to this embodiment is different in that the reference voltage that is inputted to a variable-voltage source not only changes depending on a change in the potential difference ΔV detected by a high-side potential difference detecting circuit, but also changes depending on a peak signal detected, for each frame, from the inputted video data. Hereinafter, description shall not be repeated for points which are the same as in Embodiment 1 and shall be centered on the points of difference from Embodiment 1. Furthermore, the figures applied to Embodiment 1 shall be used for figures that would otherwise overlap with those in Embodiment 1.

Hereinafter, Embodiment 2 shall be specifically described with reference to the Drawings.

FIG. **10** is a block diagram showing an outline configuration of the display device according to Embodiment 2.

A display device **100** shown in the figure includes the organic electroluminescence (EL) display unit **110**, the data line driving circuit **120**, the write scan driving circuit **130**, the control circuit **140**, a peak signal detecting circuit **150**, a signal processing circuit **160**, the high-side potential difference detecting circuit **170**, the high-side potential variable-voltage source **180**, and the monitor wire **190**.

The configuration of the organic EL display unit **110** is the same as that shown in FIG. **2** and FIG. **3** in Embodiment 1.

The peak signal detecting circuit **150** detects the peak value of the video data inputted to the display device **100**, and outputs a peak signal representing the detected peak value to the signal processing circuit **160**. Specifically, the peak signal detecting circuit **150** detects, as the peak value, data of the highest gradation level out of the video data. High gradation level data corresponds to an image that is to be displayed brightly by the organic EL display unit **110**.

The signal processing circuit **160**, which is the voltage regulating unit in this embodiment, regulates the variable-voltage source **180** to set the potential difference between the potential of the monitor pixel **111**M and the reference potential to a predetermined voltage, based on the peak signal outputted by the peak signal detecting circuit **150** and a potential difference ΔV detected by the high-side potential difference detecting circuit **170**. Specifically, the signal processing circuit **160** determines the voltage required by the organic EL element **121** and the driving transistor **125** when causing the pixels **111** to produce luminescence according to the peak signal outputted by the peak signal detecting circuit **150**. Furthermore, the signal processing circuit **160** calculates a voltage margin based on the potential difference detected by the high-side potential difference detecting circuit **170**. Subsequently, the signal processing circuit **160** sums up a voltage VEL required by the organic EL element **121**, a voltage VTFT required by the driving transistor **125**, and the voltage drop margin Vdrop, and outputs the summation result VEL+VTFT+Vdrop, as the voltage of a first reference voltage Vref**1**, to the high-side potential variable-voltage source **180**.

Furthermore, the signal processing circuit **160** outputs, to the data line driving circuit **120**, a signal voltage corresponding to the video data inputted via the peak signal detecting circuit **150**.

The high-side potential difference detecting circuit **170**, which is the voltage detecting unit in this embodiment, measures, for the monitor pixel **111**M, the high-side potential to be applied to the monitor pixel **111**M. Specifically, the high-side potential difference detecting circuit **170** measures, via the monitor wire **190**, the high-side potential to be applied to the monitor pixel **111**M. Specifically, the high-side potential difference detecting circuit **170** measures the potential at the detecting point M**1**. In addition, the high-side potential difference detecting circuit **170** measures the output potential of the high-side potential variable-voltage source **180**, and measures the potential difference ΔV between the measured high-side potential to be applied to the monitor pixel **111**M and the output potential of the high-side potential variable-voltage source **180**. Subsequently, the high-side potential difference detecting circuit **170** outputs the measured potential difference ΔV to the signal processing circuit **160**.

The high-side potential variable-voltage source **180**, which is the power supplying unit in this embodiment, outputs the high-side potential to the organic EL display unit **110**. The high-side potential variable-voltage source **180** outputs an output voltage Vout for setting the potential difference between the high-side potential of the monitor pixel **111**M and the reference potential to the predetermined potential (VEL+VTFT), according to the first reference voltage Vref**1** outputted by the signal processing circuit **160**. It is sufficient that reference potential be a potential serving as a reference in the display device **100**, and is for example a ground potential in this embodiment.

The monitor wire **190** is a high-side potential detecting line which has one end connected to the monitor pixel **111**M and the other end connected to the high-side potential difference detecting circuit **170**, and transmits the high-side potential applied to the monitor pixel **111**M to the high-side potential difference detecting circuit **170**.

Next, a brief description of the detailed configuration of the high-side potential variable-voltage source **180** shall be given.

FIG. **11** is a block diagram showing an example of a specific configuration of a high-side potential variable-voltage source according to Embodiment 2. It is to be noted that the organic EL display unit **110** and the signal processing circuit **160** which are connected to the variable-voltage source are also shown in the figure. The high-side potential variable-voltage source **180** shown in the figure is the same as the high-side potential variable-voltage source **180** described in Embodiment 1.

The error amplifier **186** compares the Vout that has been voltage-divided by the output detection unit **185** and the first reference voltage Vref**1** outputted by the signal processing circuit **160**, and outputs, to the PWM circuit **182**, a voltage that is in accordance with the comparison result. Specifically, the error amplifier **186** includes the operational amplifier **187** and the resistors R**3** and R**4**. The operational amplifier **187** has an inverting input terminal connected to the output detecting unit **185** via the resistor R**3**, a non-inverting input terminal connected to the signal processing circuit **160**, and an output terminal connected to the PWM circuit **182**. Furthermore, the output terminal of the operational amplifier **187** is connected to the inverting input terminal via the resistor R**4**. With this, the error amplifier **186** outputs, to the PWM circuit **182**, a voltage that is in accordance with the potential difference between the voltage inputted from the output detecting unit **185** and the first reference voltage Vref**1** inputted from the signal processing circuit **160**. Stated differently, the error amplifier **186** outputs, to the PWM circuit **182**, a voltage that is in accordance with the potential difference between the output voltage Vout and the first reference voltage Vref**1**.

The PWM circuit **182** outputs, to the drive circuit **183**, pulse waveforms having different duties depending on the voltage outputted by the comparison circuit **181**. Specifically, the PWM circuit **182** outputs a pulse waveform having a long ON duty when the voltage outputted by the comparison circuit **181** is large, and outputs a pulse waveform having a short ON duty when the outputted voltage is small. Stated differently, the PWM circuit **182** outputs a pulse waveform having a long ON duty when the potential difference between the output voltage Vout and the first reference voltage Vref**1** is big, and outputs a pulse waveform having a short ON duty when the potential difference between the output voltage Vout and the first reference voltage Vref**1** is small. It is to be noted that the ON period of a pulse waveform is a period in which the pulse waveform is active.

As the output voltage Vout approaches the first reference voltage Vref**1**, the voltage inputted to the PWM circuit **182** decreases, and the ON duty of the pulse signal outputted by the PWM circuit **182** becomes shorter.

Then, the time in which the switching element SW is ON becomes shorter, and the output voltage Vout gently converges with the first reference voltage Vref**1**.

The potential of the output voltage Vout, while having slight voltage fluctuations, eventually settles to a potential in the vicinity of Vout=Vref**1**.

In this manner, the high-side potential variable-voltage source **180** generates the output voltage Vout which becomes the first reference voltage Vref**1** outputted by the signal processing circuit **160**, and supplies the output voltage Vout to the organic EL display unit **110**.

Next, the operation of the aforementioned display device **100** shall be described using FIG. **12**, FIG. **13**, and FIG. **7**.

FIG. **12** is a flowchart showing the operation of the display device **100** disclosed herein.

First, the peak signal detecting circuit **150** obtains the video data for one frame period inputted to the display device **100** (step S**11**). For example, the peak signal detecting circuit **150** includes a buffer and stores the video data for one frame period in such buffer.

Next, the peak signal detecting circuit **150** detects the peak value of the obtained video data (step S**12**), and outputs a peak signal representing the detected peak value to the signal processing circuit **160**. Specifically, the peak signal detecting circuit **150** detects the peak value of the video data for each color. For example, for each of red (R), green (G), and blue (B), the video data is expressed using the 256 gradation levels from 0 to 255 (luminance being higher with a larger value). Here, when part of the video data of the organic EL display unit **110** has R:G:B=177:124:135, another part of the video data of the organic EL display unit **110** has R:G:B=24:177:50, and yet another part of the video data of the organic EL display unit **110** has R:G:B=10:70:176, the peak signal detecting circuit **150** detects **177** as the peak value of R, **177** for the peak value of G, and **176** as the peak value of B, and outputs, to the signal processing circuit **160**, a peak signal representing the detected peak value of each color.

Next, the signal processing circuit **160** determines the voltage VTFT required by the driving transistor **125** and the voltage VEL required by the organic EL element **121** when causing the organic EL element **121** to produce luminescence according to the peak values outputted by the peak signal detecting circuit **150** (step S**13**). Specifically, the signal processing circuit **160** determines the VTFT+VEL corresponding to the gradation levels for each color, using a required voltage conversion table indicating the required voltage VTFT+VEL corresponding to the gradation levels for each color.

FIG. **13** is a chart showing an example of the required voltage conversion table provided in the signal processing circuit **160**.

As shown in the figure, required voltages VTFT+VEL respectively corresponding to the gradation levels of each color are stored in the required voltage conversion table. For example, the required voltage corresponding to the peak value **177** of R is 8.5V, the required voltage corresponding to the peak value **177** of G is 9.9V, and the required voltage corresponding to the peak value **176** of B is 6.7V. Among the required voltages corresponding to the peak values of the respective colors, the largest voltage is 9.9 V corresponding to the peak value of G. Therefore, the signal processing circuit **160** determines VTFT+VEL to be 9.9V.

Meanwhile, the high-side potential difference detecting circuit **170** detects the potential at the detecting point M**1** via the monitor wire **190** (step S**14**).

Next, the high-side potential difference detecting circuit **170** receives the voltage of the output terminal **184** of the high-side potential variable-voltage source **180**, calculates the potential difference between potential at the detecting point M**1** and the reference potential, and detects the potential difference ΔV between the received potential of the output terminal **184** and the calculated potential difference (step S**15**). Subsequently, the high-side potential difference detecting circuit **170** outputs the detected potential difference ΔV to the signal processing circuit **160**. It is to be noted that the steps S**11** to S**15** up to this point correspond to the potential measuring process according to the present disclosure.

Next, the signal processing circuit **160** determines a voltage drop margin Vdrop corresponding to the potential difference ΔV detected by the high-side potential difference detecting circuit **170**, based on a potential difference signal outputted by the high-side potential difference detecting circuit **170** (step S**16**). Specifically, the signal processing circuit **160** has a voltage margin conversion table indicating the voltage drop margin Vdrop corresponding to the potential difference ΔV, and determines the voltage drop margin Vdrop with reference to the conversion table.

As shown in FIG. **7**, voltage drop margins Vdrop respectively corresponding to the potential differences ΔV are stored in the voltage margin conversion table. For example, when the potential difference ΔV is 3.4 V, the voltage drop margin Vdrop is 3.4 V. Therefore, the signal processing circuit **160** determines the voltage drop margin Vdrop to be 3.4 V.

Now, as shown in the voltage margin conversion table, the potential difference ΔV and the voltage drop margin Vdrop have an increasing function relationship. Furthermore, the output voltage Vout of the high-side potential variable-voltage source **180** rises with a bigger voltage drop margin Vdrop. In other words, the potential difference ΔV and the output voltage Vout have an increasing function relationship.

Next, the signal processing circuit **160** determines the output voltage Vout that the high-side potential variable-voltage source **180** is to be made to output in the next frame period (step S**17**). Specifically, the output voltage Vout that the high-side potential variable-voltage source **180** is to be made to output in the next frame period is assumed to be VTFT+VEL+Vdrop which is the sum value of (i) VTFT+VEL determined in the determination (step S**13**) of the voltage required by the organic EL element **121** and the driving transistor **125** and (ii) the voltage drop margin Vdrop determined in the determination (step S**15**) of the voltage margin corresponding to the potential difference ΔV.

Lastly, the signal processing circuit **160** regulates the high-side potential variable-voltage source **180** by setting the first reference voltage Vref**1** as VTFT+VEL+Vdrop at the beginning of the next frame period (step S**18**). With this, in the next frame period, the high-side potential variable-voltage source **180** supplies Vout=VTFT+VEL+Vdrop to the organic EL display unit **110**. It is to be noted that step S**16** to step S**18** correspond to the voltage regulating process according to the present disclosure.

In this manner, the display device **100** according to this embodiment includes: the high-side potential variable-voltage source **180** which outputs the high-side potential; the high-side potential difference detecting circuit **170** which measures, for the monitor pixel **111**M in the organic EL display unit **110**, (i) the high-side potential applied to the monitor pixel **111**M and (ii) the high-side potential output voltage Vout of the high-side potential variable-voltage source **180**; and the signal processing circuit **160** which regulates the high-side potential variable-voltage source **180** to set, to the predetermined potential (VTFT+VEL), the potential difference between the reference potential and the high-side potential that is applied to the monitor pixel **111**M that is measured by the high-side potential difference detecting circuit **170**. Furthermore, the high-side potential difference detecting circuit **170**, in addition, measures the high-side potential output voltage Vout of the high-side potential variable-voltage source **180**, detects the potential difference between the measured high-side potential output voltage Vout and the high-side potential applied to the monitor pixel **111**M. The signal processing circuit **160** regulates the high-side potential variable-voltage source **180** in accordance with the potential difference detected by the high-side potential difference detecting circuit **170**.

With this, the display device **100** can reduce excess voltage and reduce power consumption by detecting the voltage drop caused by the horizontal first power source wire resistance R**1***h* and the vertical first power source wire resistance R**1***v* and giving feedback to the high-side potential variable-voltage source **180** regarding the degree of such voltage drop.

Furthermore, in the display device **100**, the monitor pixel **111**M is located near the center of the organic EL display unit **110**, and thus the output voltage Vout of the high-side potential variable-voltage source **180** can be easily regulated even when the size of the organic EL display unit **110** is increased.

Furthermore, since heat generation by the organic EL element **121** is suppressed through the reduction of power consumption, the deterioration of the organic EL element **121** can be prevented.

Next, the display pattern transition in the case where the video data inputted up to the Nth frame changes from the N+1th frame onward, in the display device **100** described above, shall be described using FIG. **8** and FIG. **9**.

Initially, the video data that is assumed to have been inputted in the Nth frame and the N+1th frame shall be described.

First, it is assumed that, up to the Nth frame, the video data corresponding to the central part of the organic EL display unit **110** is a peak gradation level (R:G:B=255:255:255) in which the central part of the organic EL display unit **110** is seen as being white. On the other hand, it is assumed that the video data corresponding to a part of the organic EL display unit **110** other than the central part is a gray gradation level (R:G:B=50:50:50) in which the part of the organic EL display unit **110** other than the central part is seen as being gray.

Furthermore, from the N+1th frame onward, it is assumed that the video data corresponding to the central part of the organic EL display unit **110** is the peak gradation level (R:G:B=255:255:255) as in the Nth frame. On the other hand, it is assumed that the video data corresponding to the part of the organic EL display unit **110** other than the central part is a gray gradation level (R:G:8=150:150:150) that can be seen as a brighter gray than in the Nth frame.

Next, the operation of the display device **100** in the case where video data as described above is inputted in the Nth frame and the N+1th frame shall be described.

The potential difference ΔV detected by the high-side potential difference detecting circuit **170**, the output voltage Vout from the high-side potential variable-voltage source **180**, and the pixel luminance of the monitor pixel **111**M are shown in FIG. **8**. Furthermore, a blanking period is provided at the end of each frame period.

In time t=T**10**, the peak signal detecting circuit **150** detects the peak value of the video data of the Nth frame. The signal processing circuit **160** determines VTFT+VEL from the peak value detected by the peak signal detecting circuit **150**. Here, since the peak value of the video data of the Nth frame is R:G:B=255:255:255, the signal processing circuit **160** uses the required voltage conversion table and determines the required voltage VTFT+VEL for the N+1th frame to be, for example, 12.2V.

Meanwhile, at this time, the high-side potential difference detecting circuit **170** detects the potential at the detecting point M**1** via the monitor wire **190**, and detects the potential difference ΔV between the detected potential and the output voltage Vout outputted from the high-side potential variable-voltage source **180**. For example, in time t=T**10**, the high-side potential difference detecting circuit **170** detects ΔV=1V. Subsequently, the signal processing circuit **160** uses the voltage margin conversion table and determines the voltage drop margin Vdrop for the N+1th frame to be 1 V.

A time t=T**10** to T**11** is the blanking period of the Nth frame. In this period, an image which is the same as that in the time t=T**10** is displayed in the organic EL display unit **110**.

(a) in FIG. **9** schematically shows an image displayed on the organic EL display unit **110** in the time t=T**10** to T**11**. In this period, the image displayed on the organic EL display unit **110** corresponds to the image data of the Nth frame, and thus the central part is white and the part other than the central part is gray.

In time t=T**11**, the signal processing circuit **160** sets the voltage of the first reference voltage Vref**1** as the sum VTFT+VEL+Vdrop (for example, 13.2 V) of the determined required voltage VTFT+VEL and the voltage drop margin Vdrop.

Over a time t=T**11** to T**16**, the image corresponding to the video data of the N+1th frame is gradually displayed on the organic EL display unit **110** ((b) to (f) in FIG. **9**). At this time, the output voltage Vout from the high-side potential variable-voltage source **180** is, at all times, the VTFT+VEL+Vdrop set to the voltage of the first reference voltage Vref**1** in time t=T**11**. However, the video data corresponding to the part of the organic EL display unit **110** other than the central part is a gray gradation level that can be seen as a gray that is brighter than that in the Nth frame. Therefore, the amount of current supplied by the high-side potential variable-voltage source **180** to the organic EL display unit **110** gradually increases over time t=T**11** to T**16**, and the voltage drop in the first power source wire **112** gradually increases following this increase in the amount of current. With this, there is a shortage of power source voltage for the pixels **111** in the central part of the organic EL display unit **110**, which are the pixels **111** in a brightly displayed region. Stated differently, luminance drops below the image corresponding to the video data R:G:B=255:255:255 of the N+1th frame. Specifically, over the time t=T**11** to T**16**, the pixel luminance of the pixels **111** at the central part of the organic EL display unit **110** gradually drops.

Next, in time t=T**16**, the peak signal detecting circuit **150** detects the peak value of the video data of the N+1th frame. Here, since the detected peak value of the video data of the N+1th frame is R:G:B=255:255:255, the signal processing circuit **160** determines the required voltage VTFT+VEL for the N+2th frame to be, for example, 12.2 V.

Meanwhile, at this time, the high-side potential difference detecting circuit **170** detects the potential at the detecting point M**1** via the monitor wire **190**, and detects the potential difference ΔV between (i) the potential difference between the detected potential at the detecting point M**1** and the reference potential and (ii) and the output voltage Vout outputted from the high-side potential variable-voltage source **180**. For example, in time t=T**16**, the high-side potential difference detecting circuit **170** detects ΔV=3 V. Subsequently, the signal processing circuit **160** uses the voltage margin conversion table and determines the voltage drop margin Vdrop for the N+1th frame to be 3 V.

Next, in time t=T**17**, the signal processing circuit **160** sets the voltage of the first reference voltage Vref**1** to the sum VTFT+VEL+Vdrop (for example, 15.2 V) of the determined required voltage VTFT+VEL and the voltage drop margin Vdrop. Therefore, from time t=T**17** onward, the potential at the detecting point M**1** becomes VTFT+VEL which is the predetermined potential.

In this manner, in the display device **100**, although luminance temporarily drops in the N+1th frame, this is a very short period and thus has practically no impact on the user.

It is to be noted that although, in this embodiment, the high-side potential applied to the pixel **111**M is monitored and the high-side potential outputted from the high-side potential variable-voltage source **180** is regulated to set the potential difference between the monitored high-side potential and the reference potential to a predetermined voltage, the low-side potential applied to the pixel **111**M may be monitored and the low-side potential outputted from a low-side potential variable-voltage source may be regulated to set the potential difference between the monitored low-side potential and the reference potential to a predetermined voltage. In this case, a low-side potential difference detecting circuit is provided in place of the high-side potential difference detecting circuit **170** shown in FIG. **1**, and a low-side potential variable-voltage source is provided in place of the high-side potential variable-voltage source **180**.

A peak signal detecting circuit detects the peak value of video data inputted to the display device **100**, and outputs a peak signal indicating the detected peak value to the signal processing circuit. Specifically, the functions of such peak signal detecting circuit are the same as those of the peak signal detecting circuit **150**.

The signal processing circuit regulates the low-side potential variable-voltage source in accordance with the peak signal outputted by the peak signal detecting circuit and the potential difference ΔV detected by the low-side potential difference detecting circuit, to set the potential of the monitor pixel **111**M to a predetermined potential.

The low-side potential difference detecting circuit measures, for the monitor pixel **111**M, a low-side potential applied to the monitor pixel **111**M. In addition, the low-side potential difference detecting circuit measures the output potential of the low-side potential variable-voltage source, and measures the potential difference ΔV between (i) the potential difference between the measured low-side potential applied to the monitor pixel **111**M and the reference potential and (ii) the output potential of the low-side variable-voltage source. Subsequently, the low-side potential difference detecting circuit outputs the measured potential difference ΔV to the signal processing circuit.

The low-side potential variable-voltage source outputs the low-side potential to the organic EL display unit **110**. The low-side potential variable-voltage source outputs an output voltage Vout for setting the potential difference between the low-side potential of the monitor pixel **111**M and the reference potential to a predetermined voltage, in accordance with the reference voltage Vref outputted by the signal processing circuit. It is sufficient that reference potential be a potential serving as a reference in the display device **100**.

With this, the display device in the present disclosure can reduce excess voltage and reduce power consumption by detecting the voltage drop caused by the horizontal second power source wire resistance R**2**h and the vertical second power source wire resistance R**2**v and giving feedback to the low-side potential variable-voltage source regarding the degree of such voltage drop.

Furthermore, since heat generation by the organic EL element is suppressed through the reduction of power consumption, the deterioration of the organic EL element can be prevented.

Embodiment 3

A display device according to this embodiment is almost the same as the display device **100** according to Embodiment 2, but is different in not including the high-side potential difference detecting circuit **170** and in that the potential at the detecting point M**1** is inputted to the high-side potential variable-voltage source. Furthermore, a signal processing circuit is different in setting the voltage to be outputted to the high-side potential variable-voltage source to the required voltage VTFT+VEL. With this, in the display device according to this embodiment, the output voltage Vout of the high-side potential variable-voltage source can be regulated in real-time in accordance with the voltage drop amount, and thus, compared with Embodiment 2, the temporary drop in pixel luminance can be prevented.

FIG. **14** is a block diagram showing an outline configuration of the display device according to Embodiment 3.

A display device **200** according to the this embodiment shown in the figure is different compared to the display device **100** according to Embodiment 2 shown in FIG. **10** in not including the high-side potential difference detecting circuit **170**, and including a monitor wire **290** in place of the monitor wire **190**, a signal processing circuit **260** in place of the signal processing circuit **160**, and a high-side potential variable-voltage source **280** in place of the high-side potential variable-voltage source **180**.

The signal processing circuit **260** determines a second reference voltage Vref**2** to be outputted to the high-side potential variable-voltage source **280**, from the peak signal outputted by a peak signal detecting circuit **150**. Specifically, the signal processing circuit **260** uses the required voltage conversion table and determines the sum VTFT+VEL of the voltage VEL required by an organic EL element **121** and a voltage VTFT required by the driving transistor **125**. Subsequently, the signal processing circuit **260** sets the determined VTFT+VEL as the voltage of the second reference voltage Vref**2**.

In such manner, the second reference voltage Vref**2** that is outputted to the high-side potential variable-voltage source **280** by the signal processing circuit **260** of the display device **200** according to this embodiment is different from the first reference voltage Vref**1** that is outputted to the high-side potential variable-voltage source **180** by the signal processing circuit **160** of the display device **100** according to Embodiment 2, and is a voltage determined in accordance with the video data only. Specifically, the second reference voltage Vref**2** is not dependent on the potential difference ΔV between the potential of the output voltage Vout of the high-side potential variable-voltage source **280** and the potential at the detecting point M**1**.

The high-side potential variable-voltage source **280** measures the high-side potential applied to the monitor pixel **111**M, via the monitor wire **290**. Specifically, the high-side potential variable-voltage source **280** measures the potential at the detecting point M**1**. Subsequently, the high-side potential variable-voltage source **280** regulates the output voltage Vout in accordance with (i) the potential difference between the measured potential at the detecting point M**1** and the reference potential and (ii) the second reference voltage Vref**2** outputted by the signal processing circuit **260**.

The monitor wire **290** has one end connected to the detecting point M**1** and the other end connected to the high-side potential variable-voltage source **280**, and transmits the potential at the detecting point M**1** to the high-side potential variable-voltage source **280**.

FIG. **15** is a block diagram showing an example of a specific configuration of the high-side potential variable-voltage source **280** according to Embodiment 3. It is to be noted that the organic EL display unit **110** and the signal processing circuit **260** which are connected to the high-side potential variable-voltage source are also shown in the figure.

The high-side potential variable-voltage source **280** shown in the figure has almost the same configuration as the high-side potential variable-voltage source **180** shown in FIG. **11**, but is different in including, in place of the comparison circuit **181**, a comparison circuit **281** which compares the potential at the detecting point M**1** and the second reference voltage Vref**2**.

Here, assuming that the output potential of the high-side potential variable-voltage source **280** is Vout, and the voltage drop amount from the output terminal **184** of the high-side potential variable-voltage source **280** to the detecting point M**1** is ΔV, the potential at the detecting point M**1** is Vout−ΔV. Specifically, in this embodiment, the comparison circuit **281** compares Vref**2** and Vout−ΔV. As described above, since

Vref2=VTFT+VEL, it can be said that the comparison circuit **281** is comparing VTFT+VEL and Vout−ΔV.

On the other hand, in Embodiment 2, the comparison circuit **181** compares Vref1 and Vout. As described above, since Vref1=VTFT+VEL+ΔV, it can be said that, in Embodiment 2, the comparison circuit **181** is comparing VTFT+VEL+ΔV and Vout.

Therefore, although the comparison circuit **281** has different comparison subjects as the comparison circuit **181**, the comparison result is the same. Specifically, when the voltage drop amount from the output terminal **184** of the high-side potential variable-voltage source to the detecting point M1 is the same between Embodiment 2 and Embodiment 3, the voltage outputted by the comparison circuit **181** to the PWM circuit and the voltage outputted by the comparison circuit **281** to the PWM circuit are the same. As a result, the output voltage Vout of the high-side potential variable-voltage source **180** and the output voltage Vout of the high-side potential variable-voltage source **280** become the same. Furthermore, the potential difference ΔV and the output voltage Vout also have an increasing function relationship in Embodiment 3.

Compared to the display device **100** according to Embodiment 2, the display device **200** configured in the above manner can regulate the output voltage Vout in accordance with the potential difference ΔV between the output terminal **184** and the detecting point M1 in real-time. This is because, in the display device **100** according to Embodiment 2, the signal processing circuit **160** changes the first reference voltage Vref1 for a frame only at the beginning of each frame period. In contrast, in the display device **200** according to this embodiment, Vout can be regulated independently of the control by the signal processing circuit **260**, by inputting the voltage that is dependent on the ΔV, that is, Vout−ΔV directly to the comparison circuit **281** of the high-side potential variable-voltage source **280** without passing through the signal processing circuit **260**.

Next, the operation of the display device **200** configured in the above manner, in the case where the video data inputted up to the Nth frame changes from the N+1th frame onward, as in Embodiment 2, shall be described. It is to be noted that, as in Embodiment 2, it is assumed that, up to the Nth frame, the inputted video data is R:G:B=255:255:255 for the central part of the organic EL display unit **110** and is R:G:B=50:50:50 for the part other than the central part, and, from the N+1th frame onward, the inputted video data is R:G:B=255:255:255 for the central part of the organic EL display unit **110** and is R:G:B=150:150:150 for the part other than the central part.

FIG. **16** is a timing chart showing the operation of the display device **200** from the Nth frame to the N+2th frame.

In time t=T**20**, the peak signal detecting circuit **150** detects the peak value of the video data of the Nth frame. The signal processing circuit **260** determines VTFT+VEL from the peak value detected by the peak signal detecting circuit **150**. Here, since the peak value of the video data of the Nth frame is R:G:B=255:255:255, the signal processing circuit **260** uses the required voltage conversion table and determines the required voltage VTFT+VEL for the N+1th frame to be, for example, 12.2V.

Meanwhile, the output detecting unit **185** constantly detects the potential at the detecting point M1, via the monitor wire **290**.

Next, in time t=T**21**, the signal processing circuit **260** sets the voltage of the second reference voltage Vref2 to the determined required voltage VTFT+VEL (for example, 12.2V).

Over a time t=T**21** to T**22**, the image corresponding to the video data of the N+1th frame is gradually displayed on the organic EL display unit **110**. At this time, the amount of current supplied by the high-side potential variable-voltage source **280** to the organic EL display unit **110** gradually increases, as described in Embodiment 1. Therefore, following the increase in the amount of current, the voltage drop in the first power source wire **112** gradually increases. Specifically, the potential at the detecting point M1 gradually drops. Stated differently, the potential difference ΔV between the potential of the output voltage Vout and the potential at the detecting point M1 gradually increases.

Here, since the error amplifier **186** outputs, in real-time, a voltage that is in accordance with the potential difference between VTFT+VEL and Vout−ΔV, the error amplifier **186** outputs a voltage that causes Vout to rise in accordance with the increase in the potential difference ΔV.

Therefore, with the high-side potential variable-voltage source **280**, Vout rises in real-time in accordance with the increase in the potential difference ΔV.

This resolves the shortage of power source voltage for the pixels **111** in the central part of the organic EL display unit **110** which are the pixels **111** in the brightly displayed region. In other words, the drop in pixel luminance is resolved.

As described above, in the display device **200** according to the this embodiment, the signal processing circuit **260**, and the error amplifier **186**, the PWM circuit **182**, and the drive circuit **183** of the high-side potential variable-voltage source **280**, detect the potential difference between (i) the potential difference between the high-side potential of the monitor pixel **111**M measured by the output detecting unit **185** and the reference potential and (ii) the predetermined potential, and regulates the switching element SW in accordance with the detected potential difference. Accordingly, compared with the display device **100** according to Embodiment 2, the display device **200** according to this embodiment is able to regulate the output voltage Vout of the high-side potential variable-voltage source **280** in real-time in accordance with the voltage drop amount, and thus compared to Embodiment 2, the temporary drop in pixel luminance can be prevented.

It is to be noted that, in this embodiment, the organic EL display unit **110** is the display unit; the output detecting unit **185** is the voltage detecting unit; the signal processing circuit **260**, and the error amplifier **186**, PWM circuit **182**, and drive circuit **183** of the high-side potential variable-voltage source **280** which are surrounded by the dashed-and-single-dotted line in FIG. **15** are the voltage regulating unit; and the switching element SW, the diode D, the inductor L, and the capacitor C which are surrounded by the dashed-and-double-dotted line in FIG. **15** are the power supplying unit.

It is to be noted that, in the same manner as in Embodiment 2, in this embodiment, the low-side potential applied to the pixel **111**M may be monitored and the low-side potential outputted from a low-side potential variable-voltage source may be regulated to set the potential difference between the monitored low-side potential and the reference potential to a predetermined voltage. In this case, a low-side potential variable-voltage source is provided in place of the high-side potential variable-voltage source **180** shown in FIG. **14**, and a low-side potential variable-voltage source is provided in place of the high-side potential variable-voltage source **180**.

Embodiment 4

Embodiments 2 and 3 describe a display device which monitors the high-side or low-side potential of a single pixel to regulate, to a predetermined potential difference, the potential difference between the high-side potential and a reference potential or the potential difference between the low-side potential and the reference potential. In contrast, this embodiment describes a display device which monitors the high-side potential of a single pixel and the low-side potential of a different pixel to regulate the potential difference between the high-side potential and a reference potential A to a predetermined potential difference, and to regulate the potential difference between the low-side potential and a reference potential B to a predetermined potential difference.

Hereinafter, Embodiment 4 shall be specifically described with reference to the Drawings.

FIG. **17** is a block diagram showing an outline configuration of a display device according to Embodiment 4.

A display device **300** shown in the figure includes an organic EL display unit **310**, the data line driving circuit **120**, the write scan driving circuit **130**, the control circuit **140**, the signal processing circuit **165**, a high-side potential difference detecting circuit **170**A, a low-side potential difference detecting circuit **170**B, a high-side potential voltage margin setting unit **175**A, a low-side potential voltage margin setting unit **175**B, a high-side potential variable-voltage source **180**A, a low-side potential variable-voltage source **180**B, and monitor wires **190**A and **190**B.

Compared to the display device **50** according to Embodiment 1, the display device **300** according to this embodiment is different in including two potential difference detecting circuits, two monitor wires, and two variable-voltage sources, for the high-side potential and the low-side potential, respectively. Description of points identical to those in Embodiment 1 shall not be repeated, and only the points of difference shall be described hereafter.

FIG. **18** is a perspective view schematically showing a configuration of the organic EL display unit **310** according to Embodiment 4. It is to be noted that the lower portion of the figure is the display screen side. As shown in the figure, the organic EL display unit **310** includes the pixels **111**, the first power source wire **112**, and the second power source wire **113**. At least one predetermined pixel out of the pixels **111** is connected to the monitor wire **190**A at a high-side potential detecting point M_A. Furthermore, at least one predetermined pixel out of the pixels **111** is connected to the monitor wire **190**B at a low-side potential detecting point M_B. Hereinafter, the pixel **111** that is directly connected to the monitor wire **190**A shall be denoted as monitor pixel **111**M_A, and the pixel **111** that is directly connected to the monitor wire **190**B shall be denoted as monitor pixel **111**M_B.

The first power source wire **112** is arranged in a net-like manner to correspond to the pixels **111** that are arranged in a matrix, and is electrically connected to the high-side potential variable-voltage source **180**A disposed at the periphery of the organic EL display unit **310**. Through the outputting of a high-side power source potential from the high-side potential variable-voltage source **180**A, a potential corresponding to the high-side power source potential outputted by the high-side potential variable-voltage source **180**A is applied to the first power source wire **112**. On the other hand, the second power source wire **113** is formed in the form of a continuous film on the organic EL display unit **310**, and is connected to the low-side potential variable-voltage source **180**B disposed at the periphery of the organic EL display unit **310**. Through the outputting of a low-side power source potential from the low-side potential variable-voltage source **180**A, a potential corresponding to the low-side power source potential outputted by the low-side potential variable-voltage source **180**A is applied to the second power source wire **113**.

The optimal position of the monitor pixels **111**M_A and **111**M_B is determined depending on the wiring method of the first power source wire **112** and the second power source wire **113**, the respective values of the first power source wire resistances R1*h* and R1*v*, and the respective values of the second power source wire resistances R2*h* and R2*v*. In this embodiment, the high-side potential detecting point M_A and the low-side potential detecting point M_B are disposed in different pixels. This allows for optimization of detecting points. For example, by disposing the pixel **111**M_A in a luminescence producing region in which there is a tendency for a large high-side potential voltage drop, and disposing the pixel **111**M_B in a luminescence producing region in which there is a tendency for a large low-side potential voltage drop (rise), detecting points need not be provided in unnecessary locations and thus the total number of detecting points can be reduced.

Since a cathode electrode of an organic EL element **121** which makes up part of a common electrode included in the second power source wire **113** uses a transparent electrode (for example, ITO) having high sheet resistance, there are cases where the voltage rise amount for the second power source wire **113** is larger than the voltage drop amount for the first power source wire **112**. Therefore, by regulating in accordance with the low-side potential applied to the monitor pixel, the output potential of the power supplying unit can be regulated more appropriately, and power consumption can be further reduced.

FIG. **19**A and FIG. **19**B are circuit diagrams showing an example of a specific configuration of a pixel **111**. Specifically, FIG. **19**A is a diagram of the circuit configuration of the pixel **111**M_A connected to the high-side potential monitor wire **190**A, and FIG. **19**B is a diagram of the circuit configuration of the pixel **111**M_B connected to the low-side potential monitor wire **190**B. In the pixel **111**M_A, the monitor wire **190**A is connected to the other of the source electrode and the drain electrode of the driving element, and, in the pixel **111**M_B, the monitor wire **190**B is connected to the second electrode of the luminescence element. Specifically, each of the pixels **111**, **111**M_A, and **111**M_B includes an organic EL element **121**, a data line **122**, a scanning line **123**, a switch transistor **124**, a driving transistor **125**, and a holding capacitor **126**. At least one pixel **111**M_A is disposed in the organic EL display unit **310**, and at least one pixel **111**M_B is likewise disposed in the organic EL display unit **310**.

The functions of the respective constituent elements shown in FIG. **17** shall be described below with reference to FIG. **19**A and FIG. **19**B.

The high-side potential difference detecting circuit **170**A, which is the voltage detecting unit in this embodiment, measures, for the monitor pixel **111**M_A, the high-side potential to be applied to the monitor pixel **111**M_A. Specifically, the high-side potential difference detecting circuit **170**A measures, via the monitor wire **190**A, the high-side potential to be applied to the monitor pixel **111**M_A. In addition, the high-side potential difference detecting circuit **170**A measures the output potential of the high-side potential variable-voltage source **180**A, and measures the potential difference ΔVH between (i) the potential difference between the measured high-side potential to be applied to the monitor pixel **111**M_A and the reference potential A and (ii) the output potential of the high-side potential variable-voltage source **180**A. Subsequently, the high-side potential difference detecting circuit **170**A outputs the measured potential difference ΔVH to the high-side potential voltage margin setting unit **175**A.

The low-side potential difference detecting circuit **170**B, which is the voltage detecting unit in this embodiment, measures, for the monitor pixel **111**M_B, the low-side potential to be applied to the monitor pixel **111**M_B. Specifically, the low-side potential difference detecting circuit **170**B measures, via the monitor wire **190**B, the low-side potential to be applied to the monitor pixel **111**M_B. In addition, the low-side potential difference detecting circuit **170**B measures the output potential of the low-side potential variable-voltage source **180**B, and measures the potential difference ΔVL between (i) the potential difference between the measured low-side potential to be applied to the monitor pixel **111**M_B and the reference potential B and (ii) the output potential of the low-side variable-voltage source **180**B. Subsequently, the low-side potential difference detecting circuit **170**B outputs the measured potential difference ΔVL to the low-side potential voltage margin setting unit **175**B.

The high-side potential voltage margin setting unit **175**A, which is the high-side potential voltage regulating unit in this embodiment, regulates, based on a voltage (VEL+VTFT) at a peak gradation level and the potential difference ΔVH detected by the high-side potential difference detecting circuit **170**A, the high-side potential variable-voltage source **180**A to set the potential difference between the potential of the monitor pixel **111**M_A and the reference potential A to a predetermined potential. Specifically, the high-side potential voltage margin setting unit **175**A calculates a voltage drop margin VHdrop based on the potential difference detected by the high-side potential difference detecting circuit **170**A. Subsequently, the high-side potential voltage margin setting unit **175**A sums up the voltage (VEL+VTFT) at the peak gradation level and the voltage drop margin VHdrop, and outputs a higher voltage than the reference potential A of the summation result VEL+VTFT+VHdrop, as a first high-side potential reference voltage VHref**1**, to the high-side potential variable-voltage source **180**A.

The low-side potential voltage margin setting unit **175**B, which is the low-side potential voltage regulating unit in this embodiment, regulates, based on a voltage (VEL+VTFT) at a peak gradation level and the potential difference ΔVL detected by the low-side potential difference detecting circuit **170**B, the low-side potential variable-voltage source **180**B to set the potential difference between the potential of the monitor pixel **111**M_B and the reference potential B to a predetermined potential. Specifically, the low-side potential voltage margin setting unit **175**B calculates a voltage drop margin VLdrop based on the potential difference detected by the low-side potential difference detecting circuit **170**B. Subsequently, the low-side potential voltage margin setting unit **175**B sums up the voltage (VEL+VTFT) at the peak gradation level and the voltage drop margin VLdrop, and outputs a lower voltage than the reference potential B of the summation result VEL+VTFT+VLdrop, as a first low-side potential reference voltage VLref**1**, to the low-side potential variable-voltage source **180**B.

The high-side potential variable-voltage source **180**A, which is the power supplying unit in this embodiment, outputs the high-side potential to the organic EL display unit **310**. The high-side potential variable-voltage source **180**A outputs an output voltage VHout for setting the potential difference between the high-side potential of the monitor pixel **111**M_A and the reference potential A to the predetermined voltage (VEL+VTFT−reference potential A), according to the first high-side potential reference voltage VHref**1** outputted by the high-side potential voltage margin setting unit **175**A. It is sufficient that reference potential A be a potential serving as a reference in the display device **300**.

The low-side potential variable-voltage source **180**B, which is the power supplying unit in this embodiment, outputs the low-side potential to the organic EL display unit **310**. The low-side potential variable-voltage source **180**B outputs an output voltage VLout for setting the potential difference between the low-side potential of the monitor pixel **111**M_B and the reference potential B to the predetermined voltage (reference potential B−VEL+VTFT), according to the first low-side potential reference voltage VLref**1** outputted by the low-side potential voltage margin setting unit **175**B.

The monitor wire **190**A is a high-side potential detecting line which has one end connected to the monitor pixel **111**M_A and the other end connected to the high-side potential difference detecting circuit **170**A, and transmits the high-side potential applied to the monitor pixel **111**M_A to the high-side potential difference detecting circuit **170**A.

The monitor wire **190**B is a low-side potential detecting line which has one end connected to the monitor pixel **111**M_B and the other end connected to the low-side potential difference detecting circuit **170**B, and transmits the low-side potential applied to the monitor pixel **111**M_B to the low-side potential difference detecting circuit **170**B.

Furthermore, the configuration of the high-side potential variable-voltage source **180**A and the low-side potential variable-voltage source **180**B according this embodiment is the same as the configuration of the high-side potential variable-voltage source **180** according to Embodiment 1. In the case where the output voltage VLout of the low-side potential variable-voltage source **180**B is negative, the circuit of the low-side potential variable-voltage source **180**B is configured by changing the arrangement of the switching element SW, the diode D, the inductor L, and the capacitor C in FIG. **4**.

Furthermore, with regard to the operation of the display device **300** according to this embodiment, the operation from step S**14** to step S**18** in FIG. **5** describing the operational flow for the display device **50** in Embodiment 1 is executed in parallel for the high-side potential and the low-side potential.

According to this embodiment, the display device **300** can reduce excess voltage and reduce power consumption by detecting the voltage drop caused by the first power source wire resistance R**1**h and the first power source wire resistance R**1**v in the positive power source line-side and the voltage rise caused by the second power source wire resistance R**2**h and the second power source wire resistance R**2**v in the negative power source line-side, and giving feedback to the high-side potential variable-voltage source **180**A and the low-side potential variable-voltage source **180**A regarding the degree of such voltage drop and voltage rise, respectively.

Furthermore, since heat generation by the organic EL element **121** is suppressed through the reduction of power consumption, the deterioration of the organic EL element **121** can be prevented.

In addition, compared to the display device in Embodiment 1, in the display device **300** according to this embodiment, it is possible to set a voltage margin that takes into consideration a voltage rise that is proportionate to the wire resistance of the low-side potential power source line, and thus power consumption can be more effectively reduced in a display mode in which the voltage distribution of the low-side potential power source line is intense.

It is to be noted that in Embodiments 1 to 4, the output voltage from the variable-voltage source is regulated based on the potential difference between the voltage applied to the pixels and the voltage outputted by the variable-voltage source. In this case, the current path from the variable-voltage source to the pixels includes a wiring path outside the display region and a wiring path inside the display region in which the pixels are disposed. Specifically, in Embodiments 1 to 4, the output voltage from the variable-voltage source is regulated in accordance with the voltage drop amount both inside the display region and outside the display region, by detecting the potential difference between the voltage applied to the pixels and the voltage outputted from the variable-voltage source. In contrast, the output voltage from the variable-voltage source can be regulated in accordance with the voltage drop (rise) amount inside the display region only, by detecting the potential difference between the voltage applied to the pixels and the voltage in the wiring path outside the display region. This shall be described below using FIG. **20**A and FIG. **20**B.

FIG. **20**A is a diagram showing an outline configuration of a display panel included in a display device disclosed herein. Furthermore, FIG. **20**B is perspective diagram schematically showing the vicinity of the periphery of the display panel included in a display device disclosed herein. In FIG. **20**A, drivers such as write scan driving circuits and data line driving circuits, high-side potential power source lines, low-side potential power source lines, and flexible pads, which are interfaces for electrical connection with outside devices, are disposed in the periphery of a display panel in which pixels **111** are arranged in a matrix. Each of the high-side potential variable-voltage source and the low-side potential variable-voltage source is connected to the display panel via (i) a high-side potential power source line and flexible pads or (ii) a low-side potential power source line and flexible pads. As shown in FIG. **20**B, resistance components are also present outside the display region, and such resistance components are due to the aforementioned flexible pads, high-side potential power source lines and low-side potential power source lines. Although in Embodiments 1 to 4 described earlier, for example, the difference between the potential at the detecting point M_A and the potential of an output point Z of the high-side potential variable-voltage source is detected, the potential difference between the potential at the detecting point M_A and the potential at a connection point Y of the display panel and a high-side potential power source line may be detected for the purpose of regulating the output voltage from the variable-voltage source that is in accordance with the voltage drop amount only inside the display region. With this, the output voltage of the variable-voltage source can regulated in accordance with the voltage drop amount within the display region only. Furthermore, for the low-side potential, the potential difference between the potential at the detecting point M_B and the potential at a connection point of the display panel and a low-side potential power source line may be detected.

It is to be noted that although this embodiment describes a display device which monitors the high-side potential of one pixel and the low-side potential of a different pixel to thereby (i) regulate the potential difference between the high-side potential and the reference potential A to a predetermined potential difference and (ii) regulate the potential difference between the low-side potential and the reference potential B to a predetermined potential difference, the pixel from which the high-side potential is detected and the pixel from which the low-side potential is detected may be the same pixel. Even in such a case, the high-side potential variable-voltage source **180**A regulates the potential difference between the high-side potential and the reference potential A to a predetermined potential difference, and the low-side potential variable-voltage source **180**B regulates the potential difference between the low-side potential and the reference potential B to a predetermined potential difference.

Embodiment 5

This embodiment describes a display device that monitors the high-side potentials of plural pixels to thereby regulate, to a predetermined potential difference, the potential difference between a high-side potential specified from among the monitored high-side potentials and the reference potential.

Hereinafter, Embodiment 5 shall be specifically described with reference to the Drawings.

FIG. **21** is a block diagram showing an outline configuration of a display device according to Embodiment 5.

A display device **400** shown in the figure includes an organic EL display unit **410**, the data line driving circuit **120**, the write scan driving circuit **130**, the control circuit **140**, the peak signal detecting circuit **150**, the signal processing circuit **160**, the high-side potential difference detecting circuit **170**, the high-side potential variable-voltage source **180**, monitor wires **191**, **192**, and **193**, and a potential comparison circuit **470**.

Compared to the display device **100** according to Embodiment 2, the display device **400** according to this embodiment is different in including plural monitor wires and the potential comparison circuit **470**. Description of points identical to those in Embodiment 2 shall not be repeated, and only the points of difference shall be described hereafter.

The organic EL display unit **410** is nearly the same as the organic EL display unit **110** but is different compared to the organic EL display unit **110** in the placement of the monitor wires **191** to **193** which are provided, on a one-to-one correspondence with detecting points M**1** to M**3**, for measuring the potential at the corresponding detecting point.

The optimal position of the monitor pixels **111**M to **111**M**3** is determined depending on the wiring method of the first power source wire **112**, and the respective values of the first power source wire resistances R**1***h* and R**1***v*.

Each of the monitor wires **191** to **193** is connected to the corresponding one of the detecting points M**1** to M**3** and to the potential comparison circuit **470**, and transmits the potential at the corresponding one of the detecting points M**1** to M**3** to the potential comparison circuit **470**. With this, the potential comparison circuit **470** can measure the potentials at the detecting points M**1** to M**3** via the monitor wires **191** to **193**.

The potential comparison circuit **470** measures the potentials at the detecting points M**1** to M**3** via the corresponding ones of the monitor wires **191** to **193**. Stated differently, the potential comparison circuit **470** measures the high-side potential applied to the monitor pixels **111**M**1** to **111**M**3**. In addition, the potential comparison circuit **470** selects the lowest potential among the measured potentials at the detecting points M**1** to M**3**, and outputs the selected potential to the high-side potential difference detecting circuit **170**.

The signal processing unit **160** regulates the high-side potential variable-voltage source **180** based on the potential difference between the potential selected by the potential comparison circuit **470** and the reference potential. As a result, the high-side potential variable-voltage source **180** provides, to the organic EL display unit **410**, an output voltage Vout with which dropping of luminance does not occur in any of the monitor pixels **111**M**1** to **111**M**3**.

As described above, in the display device **400** according to this embodiment, the potential comparison circuit **470** measures the high-side potential applied to each of the pixels **111** inside the organic EL display unit **410**, and selects the lowest potential among the measured high-side potentials. In addition, the high-side potential difference detecting circuit **170** detects the potential difference ΔV between (i) the potential difference between the lowest potential selected by the potential comparison circuit **470** and the reference potential and (ii) the potential of the output voltage Vout of the high-side potential variable-voltage source **180**. Then, the signal processing circuit **160** regulates the high-side potential variable-voltage source **180** in accordance with the detected potential difference ΔV.

With this, the output voltage Vout of the high-side potential variable-voltage source **180** can be more appropriately regulated. Therefore, power consumption can be effectively reduced even when the size of the organic EL display unit is increased.

It is to be noted that, in the display device **400** according to this embodiment: the high-side potential variable-voltage source **180** is the power supplying unit; the organic EL display unit **410** is the display unit; one part of the potential comparison circuit **470** is the voltage detecting unit; and the other part of the potential comparison circuit **470**, the high-side potential difference detecting circuit **170**, and the signal processing circuit **160** are the voltage regulating unit.

Furthermore, although the potential comparison circuit **470** and the high-side potential difference detecting circuit **170** are provided separately in the display device **400**, a potential comparison circuit which compares the potential of the output voltage Vout of the variable-voltage source **180** and the potential at each of the detecting points M**1** to M**3** may be provided in place of the potential comparison circuit **470** and the high-side potential difference detecting circuit **170**.

Next, the advantageous effects produced by the display device **400** according to this embodiment shall be described.

FIG. **22** is a diagram showing potential distributions and a detecting point arrangement for the display device according to Embodiment 5. The diagram on the left side of FIG. **22** shows the potential distributions when 15 V is applied as the high-side potential power source output and 0 V, which is a grounding potential, is applied as the low-side potential power source output. Since a 1:10 ratio is assumed between the first power source wire resistance R**1***h* and the first power source resistance R**1**V, the high-side potential distribution shows a severe potential change in the vertical direction of the display panel. In contrast, since a 10:1 ratio is assumed between the second power source wire resistance R**2***h* and the second power source resistance R**2**V, the low-side potential distribution shows a small potential change over the entire display panel. In other words, the low-side potential distribution has a tendency to be approximately uniform within the display screen.

When such tendencies are present, it is possible, for example, to monitor only the potential distribution of the high-side potential which has an extremely-varying distribution, and regulate the voltage drop (rise) amount of the low-side potential based on the potential of the high-side potential. Stated in terms of the example in FIG. **22**, with respect to maximum voltage drop amount detected from the potential distribution of the high-side potential which is 3 V (15 V−12 V), the voltage drop (rise) amount of the low-side potential is considered at all times to be half (1.5 V) of such detected drop amount (3 V).

In the display panel having the characteristics shown in FIG. **22**, a significant error does not occur even when the above-described voltage drop (rise) amount of the low-side potential is not measured, and thus, as a result, there is the advantage of obtaining a power conservation effect while reducing the detecting points for the low-side potential. Specifically, even without measuring the high-side potential and the low-side potential at each of the set pixels **111**M**1** to **111**M**3**, it is sufficient to measure only the high-side potential at each of the pixels **111**M**1** to **111**M**3**, and thus the detecting points are reduced from six points to three points. With this, the design of the interior of the display panel which requires consideration to the arrangement of monitor wires is simplified and picture quality deterioration due to monitor wire addition can be avoided.

In addition, since monitor wires for the low-side potential are eliminated, in a panel format in which light is emitted from the side at which the low-side potential is detected, there is the advantage that line defects originating from the monitor lines are not readily visible.

It is to be noted that although the three detecting points M**1** to M**3** are illustrated in the figure, having plural detecting points is sufficient, and it is sufficient to determine the optimal positioning and number of points based on the method of wiring of the power source wires and the value of the wire resistance.

Although the display device according to the present disclosure has been described thus far based on the embodiments, the display device according to the present disclosure is not limited to the above-described embodiments. Modifications that can be obtained by executing various modifications to Embodiments 1 to 5 that are conceivable to a person of ordinary skill in the art without departing from the essence of the present disclosure, and various devices internally equipped with the display device according to the present disclosure are included in the present disclosure.

For example, the drop in the pixel luminance of the pixel to which the monitor wire inside the organic EL display unit is provided may be compensated.

FIG. **23** is a graph showing the pixel luminance of a normal pixel and the pixel luminance of a pixel having the monitor wire, which correspond to the gradation levels of video data. It is to be noted that a normal pixel refers to a pixel among the pixels of the organic EL display unit, other than the pixel provided with a monitor wire.

As is clear from the figure, when the gradation levels of the video data are the same, the luminance of the pixel having the monitor wire drops more than the luminance of the normal pixel. This is because, with the provision of a monitor wire, the capacitance value of the holding capacitor **126** of the pixel decreases. Therefore, even when video data which causes luminance to be produced with the same luminance evenly throughout the entirety of the organic EL display unit is inputted, the image to be displayed on the organic EL display unit is an image in which the luminance of the pixels having a monitor wire is lower than the luminance of the other pixels. In other words, line defects occur. FIG. **24** is a diagram schematically showing an image in which line defects occur.

In order to prevent line defects, the display device may correct the signal voltage applied to the organic EL display unit from the data line driving circuit **120**. Specifically, since the positions of the pixels having a monitor wire are known at the time of designing, it is sufficient to pre-set the signal voltage to be provided to the pixels in such locations to be higher by the amount of drop in luminance. With this, it is possible to prevent line defects caused by the provision of monitor wires.

Furthermore, although the signal processing circuit has the required voltage conversion table indicating the required voltage VTFT+VEL corresponding to the gradation levels of each color, the signal processing circuit may have, in place of the required voltage conversion table, the current-voltage characteristics of the driving transistor **125** and the current-voltage characteristics of the organic EL element **121**, and determine VTFT+VEL by using these two current-voltage characteristics.

FIG. **25** is a graph showing together current-voltage characteristics of the driving transistor and current-voltage characteristics of the organic EL element. In the horizontal axis, the direction of dropping with respect to the source potential of the driving transistor is the normal direction.

In the figure, current-voltage characteristics of the driving transistor and current-voltage characteristics of the organic EL element which correspond to two different gradation levels are shown, and the current-voltage characteristics of the driving transistor corresponding to a low gradation level is indicated by Vsig**1** and the current-voltage characteristics of the driving transistor corresponding to a high gradation level is indicated by Vsig**2**.

In order to eliminate the impact of display defects due to changes in the source-to-drain voltage of the driving transistor, it is necessary to cause the driving transistor to operate in the saturation region. On the other hand, the pixel luminescence of the organic EL element is determined according to the drive current. Therefore, in order to cause the organic EL element to produce luminescence precisely in accordance with the gradation level of video data, it is sufficient that the voltage remaining after the drive voltage (VEL) of the organic EL element corresponding to the drive current of the organic EL element is deducted from the voltage between the source electrode of the driving transistor and the cathode electrode of the organic EL element is a voltage that can cause the driving transistor to operate in the saturation region. Furthermore, in order to reduce power consumption, it is preferable that the drive voltage (VTFT) of the driving transistor be low.

Therefore, in FIG. **25**, the organic EL element produces luminescence precisely in accordance with the gradation level of the video data and power consumption can be reduced most with the VTFT+VEL that is obtained through the characteristics passing the point of intersection of the current-voltage characteristics of the driving transistor and the current-voltage characteristics of the organic EL element on the line indicating the boundary between the linear region and the saturation region of the driving transistor.

In this manner, the required voltage VTFT+VEL corresponding to the gradation levels for each color may be calculated using the graph shown in FIG. **25**.

With this, power consumption can be further reduced.

It is to be noted that although the respective display devices according to Embodiments 2, 3, and 5 have a configuration in which a peak signal detecting circuit is provided, taken from the viewpoint of operating the driving transistor in the saturation region, it is possible to cause the organic EL element to produce luminescence precisely even without the peak signal detecting circuit, by storing the voltage (VTFT+VEL) at the peak gradation level in a memory beforehand, as in Embodiments 1 and 4, and setting the voltage (VTFT+VEL) as the reference voltage at all times.

Furthermore, in Embodiment 1, the voltage margin setting unit **175** outputs, to the high-side potential variable-voltage source **180**, the reference voltage Vref**1**A to which the potential difference ΔV detected by the high-side potential difference detecting circuit **170** has been added. In contrast, the display device **50** according to Embodiment 1 may be configured without a potential difference detecting circuit and with the potential of the detecting point M1 being inputted directly to the high-side potential variable-voltage source **180**, as in the display device **200** according to Embodiment 3. Even with this configuration, it is possible to produce the same advantageous effects as with the display device **50** according to Embodiment 1.

Furthermore, in Embodiment 4, the high-side potential voltage margin setting unit **175**A outputs, to the high-side potential variable-voltage source **180**A, the reference voltage VHref**1** to which the potential difference ΔVH detected by the high-side potential difference detecting circuit **170**A has been added, and the low-side potential voltage margin setting unit **175**B outputs, to the low-side potential variable-voltage source **180**B, the reference voltage VLref**1** to which the potential difference ΔVL detected by the low-side potential difference detecting circuit **170**B has been added. In contrast, the display device **300** according to Embodiment 4 may be configured without a high-side potential difference detecting circuit and low-side potential difference detection circuit and with the potentials of the detecting point M_A and detecting point M_B being inputted directly to the high-side potential variable-voltage source **180**A and the low-side potential variable-voltage source **180**A, as in the display device **200** according to Embodiment 3 Even with this configuration, it is possible to produce the same advantageous effects as with the display device **50** according to Embodiment 1.

Furthermore, in Embodiments 5, the voltage regulating unit may detect the potential difference between (i) the potential difference between the low-side potential of the monitor pixels measured by the voltage detection unit and the reference potential and (ii) the predetermined voltage, and regulate the power supplying unit in accordance with the detected potential difference.

Furthermore, in Embodiment 2, the signal processing circuit may change the first reference voltage Vref**1** on a plural frame (for example, a 3-frame) basis instead of changing the first reference voltage Vref**1** on a per frame basis.

With this, the power consumption occurring in the high-side potential variable-voltage source **180** can be reduced because the potential of the first reference voltage Vref**1** fluctuates.

Furthermore, the signal processing circuit may measure the potential differences outputted from the potential difference detecting circuit and the potential comparison circuit over plural frames, average the measured potential differences, and regulate the variable-voltage source in accordance with the average potential difference. Specifically, the process of detecting the potential at the detecting point (step S**14**) and the process of detecting the potential difference (step S**15**) in the flowchart shown in FIG. **12** may be executed over plural frames, and the potential differences for the plural frames detected in the process of detecting the potential difference (step S**15**) may be averaged in the process of determining the voltage margin (step S**16**), and the voltage margin may be determined in accordance with the average potential difference.

Furthermore, the signal processing circuit may determine the first reference voltage Vref**1** and the second reference voltage Vref**2** with consideration being given to an aged deterioration margin for the organic EL element **121**. For example, assuming that the aged deterioration margin for the organic EL element **121** is Vad, the signal processing circuit **160** may determine the voltage of the first reference voltage Vref**1** to be VTFT+VEL+Vdrop+Vad, and the signal processing circuit **260** may determine the voltage of the second reference voltage Vref**2** to be VTFT+VEL+Vad.

Furthermore, although the switch transistor **124** and the driving transistor **125** are described as being P-type transistors in the above-described embodiments, they may be configured of N-type transistors.

Furthermore, although the switch transistor **124** and the driving transistor **125** are TFTs, they may be other field-effect transistors.

Furthermore, the processing units included in the display devices **50**, **100**, **200**, **300**, and **400** according to the above-described embodiments are typically implemented as an LSI which is an integrated circuit. It is to be noted that part of the processing units included in the display devices **50**, **100**, **200**, 300, and 400 can also be integrated in the same substrate as the organic EL display units 110, 310, and 410. Furthermore, they may be implemented as a dedicated circuit or a general-purpose processor. Furthermore, a Field Programmable Gate Array (FPGA) which allows programming after LSI manufacturing or a reconfigurable processor which allows reconfiguration of the connections and settings of circuit cells inside the LSI may be used.

Furthermore, part of the functions of the data line driving circuit, the write scan driving circuit, the control circuit, the peak signal detecting circuit, the signal processing circuit, and the potential difference detecting circuit included in the display devices 50, 100, 200, 300, and 400 according to the exemplary embodiments may be implemented by having a processor such as a CPU execute a program. Furthermore, the exemplary embodiments may also be implemented as a display device driving method including the characteristic steps implemented through the respective processing units included in the display devices 50, 100, 200, 300, and 400.

Furthermore, although the foregoing descriptions exemplify the case where the display devices 50, 100, 200, 300, and 400 are active-matrix organic EL display devices, one or more exemplary embodiments may be applied to organic EL display devices other than that of the active-matrix type, and may be applied to a display device other than an organic EL display device using a current-driven luminescence element, such as a liquid crystal display device.

Furthermore, for example, a display device according to the present disclosure is built into a thin flat-screen TV such as that shown in FIG. 26. A thin, flat TV capable of high-accuracy image display reflecting a video signal is implemented by having the display device according to the present disclosure built into the TV.

Each of the structural elements in each of the above-described embodiments may be configured in the form of an exclusive hardware product, or may be realized by executing a software program suitable for the structural element. Each of the structural elements may be realized by means of a program executing unit, such as a CPU and a processor, reading and executing the software program recorded on a recording medium such as a hard disk or a semiconductor memory.

The herein disclosed subject matter is to be considered descriptive and illustrative only, and the appended Claims are of a scope intended to cover and encompass not only the particular embodiment(s) disclosed, but also equivalent structures, methods, and/or uses.

INDUSTRIAL APPLICABILITY

One or more exemplary embodiments described herein are particularly useful as an active-type organic EL flat panel display.

The invention claimed is:

1. A display device, comprising:

a power supply configured to output at least one of a high-side output potential and a low-side output potential;

a display in which pixels are arranged and which receives power supply from the power supply;

a voltage detector configured to detect at least one of a high-side applied potential to be applied to at least one of the pixels in the display and a low-side applied potential to be applied to at least one of the pixels in the display which is the same as or different from the at least one of the pixels to which the high-side applied potential is to be applied;

a voltage regulator configured to regulate at least one of the high-side output potential and the low-side output potential outputted by the power supply to set, to a predetermined potential difference, a potential difference between (i) at least one of the high-side applied potential and the low-side applied potential and (ii) a reference potential; and

at least one of:

a high-side potential detecting line having one end connected to the at least one pixel for which the high-side applied potential is detected and the other end connected to the voltage detector, for transmitting the high-side applied potential to the voltage detector; and

a low-side potential detecting line having one end connected to the at least one pixel for which the low-side applied potential is detected and the other end connected to the voltage detector, for transmitting the low-side applied potential to the voltage detector.

2. The display device according to claim 1,

wherein the at least one pixel for which the high-side applied potential is detected and the at least one pixel for which the low-side applied potential is detected are different pixels.

3. The display device according to claim 1,

wherein at least one of (i) the at least one pixel for which the high-side applied potential is detected and (ii) the at least one pixel for which the low-side applied potential is detected is plural in number.

4. The display device according to claim 3,

wherein the voltage regulator is configured to:

select at least one applied potential from:

a lowest applied potential among high-side applied potentials detected by the voltage detector; and

a highest applied potential among low-side applied potentials detected by the voltage detector; and

regulate the power supply based on the selected at least one applied potential.

5. The display device according to claim 1,

wherein the voltage detector is further configured to detect at least one of the high-side output potential and the low-side output potential which are outputted by the power supply, and

the voltage regulator is configured to regulate at least one of the high-side output potential and the low-side output potential which are outputted by the power supply, in accordance with a first potential difference which is at least one of (i) a potential difference between the high-side output potential and the high-side applied potential and (ii) a potential difference between the low-side output potential and the low-side applied potential.

6. The display device according to claim 5,

wherein the voltage regulator is configured to perform the regulation that realizes an increasing function relationship between (i) at least one of a potential difference between the high-side output potential and the reference potential and a potential difference between the low-side output potential and the reference potential and (ii) the first potential difference.

7. The display device according to claim 1,

wherein the voltage detector is further configured to detect at least one of (i) a potential in a high-side potential current path connecting the power supply and a high potential side of the pixels and (ii) a potential in a low-side potential current path connecting the power supply and the low potential side of the pixels; and

the voltage regulator is configured to regulate at least one of the high-side output potential and the low-side output potential that are outputted by the power supply, in accordance with a second potential difference which is at least one of (i) a potential difference between the potential in the high-side potential current path and the high-side applied potential and (ii) a potential difference between the potential in the low-side potential current path and the low-side applied potential.

8. The display device according to claim **7**,

wherein the voltage regulator is configured to perform the regulation that realizes an increasing function relationship between (i) at least one of a potential difference between the high-side output potential and the reference potential and a potential difference between the low-side output potential and the reference potential and (ii) the second potential difference.

9. The display device according to claim **1**,

wherein each of the pixels includes:

a driving element having a source electrode and a drain electrode; and

a luminescence element having a first electrode and a second electrode, the first electrode being connected to one of the source electrode and the drain electrode of the driving element,

the high-side applied potential is applied to one of the second electrode and the other of the source electrode and the drain electrode, and

the low-side applied potential is applied to the other of the second electrode and the other of the source electrode and the drain electrode.

10. The display device according to claim **9**,

wherein the pixels are arranged in rows and columns,

the display further comprises a first power source line and a second power source line, the first power source line connecting the others of the source electrode and the drain electrode of the respective driving elements of adjacent pixels in at least one of the row direction and the column direction, and the second power source line connecting the second electrodes of the respective luminescence elements of adjacent pixels in the row direction and the column direction, and

the pixels receive power from the power supply via the first power source line and the second power source line.

11. The display device according to claim **10**,

wherein the second electrode and the second power source line are part of a common electrode that is common to the pixels, and are electrically connected to the power supply so that a potential is applied to the common electrode from a periphery of the common electrode.

12. The display device according to claim **11**,

wherein the second electrode comprises a transparent conductive material including a metal oxide.

13. The display device according to claim **9**,

wherein the luminescence element is an organic electroluminescence (EL) element.

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